

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1	23/9/15	INTRODUCTION	I.	Black Board		
2	24/9/15	DESIGN OF DIGITAL SYSTEMS :		"		
3,4	25/9/15 28/9/15	ASM charts		"		
5	30/9/15	Hardware description language		"		
6	1/10/15			"		
7	2/10/15	Control Sequence method		"		
8	5/10/15			"		
9	7/10/15	Reduction of State tables.		"		
10	8/10/15			"		
11	9/10/15	State assignments.		"		
12	12/10/15			"		
13	14/10/15	INTRODUCTION	II.	"		
14	17/10/15			"		
15	19/10/15	Design of combinational circuits		"		
16	20/10/15	Design of combinational circuits		"		
17	23/10/15	Design of iterative circuits		"		
18	26/10/15	Design of sequential circuits using Karnaugh maps		"		
19	29/10/15	Design of sequential circuits using Karnaugh maps		"		
20	31/10/15	Sequential design using PLD, FPGA's		"		
21	4/11/15			"		
22	5/11/15	INTRODUCTION	III.	"		
23	6/11/15	FAULT MODELING		"		
24		fault classes and models.		"		
25	9/11/15	Stuck at faults		"		
		Bridging faults		"		
26	10/11/15	Transition and intermittent faults		"		
		and fault detection experiment.		"		

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28	12/11/15	Machine identification		Blackboard		
29	13/11/15	Design of fault detection experiment		"		
30	23/11/15	INTRODUCTION	<u>IV</u>	"		
31	25/11/15	TEST GENERATION		"		
32	26/11/15	fault diagnosis of combinational circuits by conventional methods		"		
33	27/11/15	Path Sensitization technique.		"		
34	28/11/15	Boolean difference method				
35	1/12/15	Kohavi algorithm		"		
36	3/12/15	TEST PATTERN GENERATION		"		
37	4/12/15	PODEM		"		
38	7/12/15	D-algorithm		"		
39	9/12/15	PODEM		"		
40	10/12/15	PODEM		"		
41	11/12/15	Random testing		"		
42	12/12/15	Transition Count testing		"		
43	14/12/15	Signature analysis		"		
44	17/12/15	Testing for bridging faults.		"		
45	18/12/15	INTRODUCTION	<u>V</u>	"		
46	21/12/15	PROGRAMMING LOGIC ARRAYS.		"		
47	23/12/15	Design using PLA's		"		
48	24/12/15	PLA design.		"		

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51	31/12/15	PLA TESTING		Blackboard		
52	4/1/16	Fault models		"		
		Test generation		"		
		Testable PLA design		"		
53	5/1/16	INTRODUCTION	VI	"		
54	6/1/16	ASYNCHRONOUS SEQUENTIAL MACHINE		"		
		-fundamental mode model		"		
55	7/1/16	flow table		"		
56	8/1/16	State reduction		"		
57	10/1/16	minimal closed covers		"		
58	20/1/16	Races		"		
59	24/1/16	Cycles and		"		
	24/1/16	Hazards.		"		
60	22/1/16	Revision		"		