**COURSE STRUCTUREAND SYLLABI**

**FOR**

**M.TECH**

**VLSI SYSTEM DESIGN**

**From The Academic Year 2016 – 2017**

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**ADITYA Institute of Technology And Management**

***(An Autonomous Institution)***

**Approved by AICTE, Permanently Affiliated to JNTUK, Kakinada**

**Accredited by NBA & NAAC, Recognized by UGC under 2(f) & 12(b)**

**K. Kotturu, TEKKALI – 532 201, Srikakulam Dist., A.P.,**

**ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI**

***(An Autonomous Institution)***

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**COURSE STRUCTURE (AR16)**

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| **M. Tech. (VLSI System Design) – 1st SEMESTER** | | | | | | | | |
| **S. No.** | **SUBJECT**  **CODE** | **SUBJECT** | **L** | **P** | **C** | **MARKS** | | |
| **INT** | **EXT** | **TOTAL** |
| 1 | 16MVL1001 | Digital System Design& Testing | 4 | - | 4 | 40 | 60 | 100 |
| 2 | 16MVL1002 | Digital Design Through HDL | 4 | - | 4 | 40 | 60 | 100 |
| 3 | 16MVL1003 | Analog IC Design | 4 | - | 4 | 40 | 60 | 100 |
| 4 | 16MVL1004 | Digital IC Design | 4 | - | 4 | 40 | 60 | 100 |
| 5 |  | ***Elective - I*** |  |  |  |  |  |  |
| 16MVL1005 | a) Embedded System Design | 4 | - | 4 | 40 | 60 | 100 |
| 16MVL1006 | b) Semiconductor Devices Modeling |
| 6 |  | ***Elective - II*** |  |  |  |  |  |  |
| 16MVL1007 | a) Hardware & Software Co-design | 4 | - | 4 | 40 | 60 | 100 |
| 16MVL1008 | b) Embedded and Real time systems |
| 7 | 16MVL1101 | HDL Programming Laboratory | - | 4 | 2 | 40 | 60 | 100 |
|  | | TOTAL | 24 | 4 | 26 | 280 | 420 | 700 |

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| **M. Tech. (VLSI System Design) – 2nd SEMESTER** | | | | | | | | |
| **S. No.** | **SUBJECT**  **CODE** | **SUBJECT** | **L** | **P** | **C** | **MARKS** | | |
| **INT** | **EXT** | **TOTAL** |
| 1 | 16MVL1009 | Mixed Signal IC design | 4 | - | 4 | 40 | 60 | 100 |
| 2 | 16MVL1010 | Algorithms for VLSI Design Automation | 4 | - | 4 | 40 | 60 | 100 |
| 3 | 16MVL1011 | Low Power VLSI Design | 4 | - | 4 | 40 | 60 | 100 |
| 4 | 16MVL1012 | Design of Fault Tolerant Systems | 4 | - | 4 | 40 | 60 | 100 |
| 5 |  | ***Elective – III*** |  |  |  |  |  |  |
| 16MVL1013 | a) VLSI Signal Processing | 4 | - | 4 | 40 | 60 | 100 |
| 16MVL1014 | b) System Modeling & Simulation |
| 6 |  | ***Elective – IV*** |  |  |  |  |  |  |
| 16MVL1015 | a) CPLD and FPGA Architecture and Applications | 4 | - | 4 | 40 | 60 | 100 |
| 16MVL1016 | System on Chip (SOC) Design |
| 7 | 16MVL1102 | Mixed Signal simulation Lab | - | 4 | 2 | 40 | 60 | 100 |
|  | | TOTAL | 24 | 4 | 26 | 280 | 420 | 700 |

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| --- | --- | --- | --- | --- | --- | --- | --- |
| **M. Tech. (VLSI) – 3rd SEMESTER** | | | | | | | |
| **S. No.** | **SUBJECT**  **CODE** | **SUBJECT** | **L** | **P** | **C** | **Marks** | |
| **I** | **E** |
| 1 | 16MVL2201 | Technical Seminar | - | - | 2 | 100 | - |
| 2 | 16MVL2202 | Project Work | - | - | 12 | - | - |
| TOTAL | | | - | | 14 | 100 | |

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| **M. Tech. (VLSI) – 4th SEMESTER** | | | | | | | |
| **S. No.** | **SUBJECT**  **CODE** | **SUBJECT** | **L** | **P** | **C** | **Marks** | |
| **I** | **E** |
| 1 | 16MVL2203 | Project Work | - | - | 14 | - | - |
| TOTAL | | | - | | 14 |  | |

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – I Sem.**

**DIGITAL SYSTEM DESIGN & TESTING**

**(Common to M. Tech. VLSI and DECS)**

**Subject Code : 16MVL1001 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives**

The main objective of this course is to

1. Explain the designing principles of various digital systems
2. Analyze a given digital system and decompose it into logical blocks involving both combinational and sequential circuit elements.
3. Explain Reduction of state tables and state assignments.
4. Describe the Fault Modeling and Test pattern Generation methods.
5. Describe PLA minimization and testing.

**Outcomes**

Student will be able to

1. Apply knowledge of digital systems, Sequential Circuit Design and design of digital logic circuits
2. Explain fault modeling and classes.
3. Apply knowledge of different algorithms for generating test patterns.
4. Detect states and faults in sequential circuits.
5. Explain PLA minimization and testing.
6. Analyze an asynchronous sequential machines

**UNIT – I**

DESIGN OF DIGITAL SYSTEMS: ASM charts, Data path design and Control Logic implementation, Reduction of state tables, State assignments.

**UNIT – II**

SEQUENTIAL CIRCUIT DESIGN: Design of Iterative circuits, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLD, FPGAs.

**UNIT – III**

FAULT MODELING: Fault classes and models – Stuck at faults, bridging faults, transition and intermittent faults.

TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

**UNIT – IV**

TEST PATTERN GENERATION: D – algorithm, PODEM, Random testing, transition count testing, Signature analysis and testing for bridging faults.

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: State identification, Machine identification, and fault detection experiment.

**UNIT – V**

PROGRAMMING LOGIC ARRAYS: Design using PLA’s, PLA minimization and PLA folding.

PLA TESTING: Fault models, Test generation and Testable PLA design.

**UNIT – VI**

ASYNCHRONOUS SEQUENTIAL MACHINE: fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

**TEXT BOOKS:**

1. Z. Kohavi – “Switching & finite Automata Theory” (TMH).

2. N. N. Biswas – “Logic Design Theory” (PHI).

3. Nolman Balabanian, Bradley Calson – “Digital Logic Design Principles” – Wily Student Edition

2004.

**REFRENCE BOOKS:**

1. M. Abramovici, M. A. Breues, A. D. Friedman – “Digital System Testing and Testable Design”,

Jaico Publications.

2. Charles H. Roth Jr. – “Fundamentals of Logic Design”.

3. Frederick. J. Hill & Peterson – “Computer Aided Logic Design” – Wiley 4th Edition.

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – I Sem.**

**DIGITAL DESIGN THROUGH HDL**

**(Common to M. Tech. VLSI and DECS)**

**Subject Code : 16MVL1002 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives**

1. Learn the design and implement of the fundamental digital logic circuits using Verilog hardware description language.
2. Find the design issues of system on chip.
3. Write the Verilog & VHDL Programming for combinational and sequential circuits using different styles of modeling.
4. Design large Systems using tasks and functions.
5. Design large systems using packages and libraries.

**Outcomes**

1. Design and implement the fundamental digital logic circuits using Verilog & VHDL at various levels of abstractions.
2. Write the Test bench simulation programs for all logic circuits.
3. Use the tasks and functions in digital system design process.
4. Design a large digital systems based on small modules.
5. Analyze the timing parameters of simulation and synthesis process.

**UNIT I:**

INTRODUCTION TO VERILOG : ASIC Design flow, FPGA Design flow, comparison between ASIC Design flow and FPGA Design flow, Features of Verilog HDL, different Levels of Design Description, Simulation, Test bench Simulation and Synthesis process,

LANGUAGE ELEMENTS OF VERILOG HDL: Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators, System Tasks, Exercises.

**UNIT II:**

GATE LEVEL MODELING : Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flip flops with Gate Primitives, Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits, Exercises.

**UNIT III:**

BEHAVIORAL MODELING : Introduction, Operations and Assignments, Functional Bifurcation, Initial Construct, Always Construct, Examples, Assignments with Delays, Wait construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non blocking Assignments, The case statement, Simulation Flow. iƒ and iƒ-else constructs, assign-deassign construct, repeat construct, for loop, the disable construct, while loop, forever loop, parallel blocks, force-release construct, Event.

**UNIT IV:**

MODELING AT DATA FLOW LEVEL: Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators. Verilog HDL programming for different combinational and sequential circuits.

SYSTEM TASKS, FUNCTIONS, AND COMPILER DIRECTIVES : Introduction, Parameters, Path Delays, Module Parameters, System Tasks and Functions, File-Based Tasks and Functions, Compiler Directives, Hierarchical Access, General Observations, Exercises, Function, Tasks, FSM Design (Moore and Mealy Machines)

**UNIT V:**

INTRODUCTIONTO VHDL: BASIC LANGUAGE ELEMENTS: Identifiers, Data Objects, Data Types, Operators.

BEHAVIORAL MODELING: Entity Declaration, Architecture Body, Process Statement, Variable Assignment Statement, Signal Assignment Statement, Wait Statement, If Statement, Case Statement, Null Statement, Loop Statement.

DATAFLOW MODELING: Concurrent Signal Assignment Statement, Concurrent versus Sequential Signal Assignment, Conditional Signal Assignment Statement.

**UNIT VI:**

STRUCTURAL MODELING: Component Declaration, Component Instantiation, Examples, Resolving Signal Values.

GENERICS AND CONFIGURATIONS: Generics, Configuration Specification, Configuration Declaration.

PACKAGES AND LIBRARIES: Package Declaration, Package Body, Design Libraries, Design File.

**Text Books:**

1. Design through Verilog HDL – T.R. Padmanabhan and B. Bala Tripura Sundari, WSE, 2004

IEEEP press.

2. A Verilog Primer – J. Bhaskar, BSP, 2003.

3. A VHDL Primer - J. Bhaskar, PHI, 3rd edition

**Reference Books:**

1. Fundamentals of Logic Design with Verilog – Stephen. Brown and Zvonko Vranesic, TMH, 2005.

2. Digital Systems Design using VHDL – Charles H Roth, Jr. Thomson Publications, 2004.

3. Advanced Digital Design with Verilog HDL – Michael D. Ciletti, PHI, 2005.

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – I Sem.**

**ANALOG IC DESIGN**

**Subject Code : 16MVL1003 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives**

1. To provide theoretical basics for analysis and design of analog integrated circuits.
2. To understand various current mirror configurations in application to different amplifiers.
3. To understand various advanced current mirror configurations and comparators.
4. To introduce PLL concept in integrated circuits.
5. To understand switched capacitor circuits for realizing analog signal processing in MOS integrated circuits.
6. To introduce Nyquist data converters useful in many applications.

**Outcomes**

1. Design two stage CMOS operational amplifiers and compensation techniques.
2. Illustrate current mirror circuits in single stage CMOS operational amplifiers.
3. Illustrate advanced current mirrors and comparators.
4. Understand PLL use in integrated circuits
5. Understand switched capacitor circuits.
6. Design and analyze CMOS A/D and D/A data converters of different types.

**UNIT – I**

BASIC OPERATIONAL AMPLIFIER DESIGN AND COMPENSATION: General considerations one – state op-amps, Two Stage CMOS Operational Amplifier, opamp gain, frequency response, slew rate, systematic offset voltage, Feedback and Operational Amplifier Compensation-linear settling time, opamp compensation, compensating the two stage opamp, lead compensation, compensation independent of process and temperature.

**UNIT – II**

CURRENT MIRRORS AND SINGLE STAGE AMPLIFIERS: Simple COMS, BJT current mirror, Cascode Wilson Wilder current mirrors. Common Source amplifier source follower, common gate amplifier

**NOISE**: Types of Noise – Thermal Noise-flicker noise- Noise in opamps- Noise in common source stage noise band width.

**UNIT – III**

ADVANCED CURRENT MIRRORS & COMPARATORS: Advanced Current Mirrors, Folded-Cascode Operational Amplifier, Current Mirror Operational Amplifier, Linear settling time revisited, Fully Differential Operational Amplifier. Common Mode Feedback Circuits, Current Feedback Operational Amplifier.

**UNIT – IV**

PHASED LOCKED LOOP DESIGN: PLL concepts- The phase locked loop in the locked condition Integrated circuit PLLs– phase Detector- Voltage controlled oscillator case study: Analysis of the 560 B Monolithic PLL.

**UNIT – V**

SWITHCHED CAPACITORS CIRCUITS: Basic Building blocks op-amps capacitors switches – non-over lapping clocks-Basic operations and analysis-resistor equivalence of la switched capacitor-parasitic sensitive integrator parasitic insensitive integrators signal flow graph analysis-First order filters- switch sharing fully differential filters – charged injections-switched capacitor gain circuits parallel resistor –capacitor circuit – preset table gain circuit –other switched capacitor circuits – full wave rectifier – peak detector sinusoidal oscillator.

**UNIT – VI**

COMPARATORS: Using an op-amp for comparator-charge injection errors- latched comparator.

NYQUIST RATE D/A CONVERTERS: Decoder based converter resistor storing converters folded resister string converter –Binary scale converters – Binary weighted resistor converters – Reduced resistance ratio ladders – R-2R based converters – Thermometer code current mode D/A converters.

NYQUIST RATE A/D CONVERTERS: Integrating converters – successive approximation converters. DAC based successive approximation – flash converters time interleaved A/D converters.

**TEXT BOOKS:**

1. Analog Integrated circuit Design by David A Johns, Ken Martin, John Wiley & Sons.

2. Analysis and design of Analog Integrated Circuits, by Gray, Hurst Lewis, Meyer. John Wiley & Sons.

3. Design of Analog CMOS Integrated Circuits, Behzad Razavi, TMH

4. Gregolian & Temes, “Analog MOS Integrated Circuits”, John Wiley, 1986.

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – I Sem.**

**DIGITAL IC DESIGN**

**Subject Code : 16MVL1004 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives**

1. Comprehend the different issues related to the development of digital Integrated circuits including fabrication, circuit design, implementation Methodologies, testing, design methodologies and tools and future Trends.
2. Understanding the main principles of various Digital building blocks used in IC design.
3. To know the design processes of MOS and CMOS circuits by studying MOS layers, Stick diagrams, Layout diagrams
4. To design of various Combinational Logic circuits like Manchester, Carry select and Carry Skip adders, Crossbar and barrel shifters, Multiplexer and various circuits for Static and Dynamic RAM.
5. To understand the design of D flips flop using Transmission gates and the design of NOR and NAND based ROM Memory.

**Outcomes**

**At the end of the course the student will be:**

1. Able To Understand The Concepts of MOS Transistor and the CMOS Inverter.
2. Able to understand the concepts and designing of digital building blocks like combinational logic circuits, sequential logic circuits using VHDL.
3. Able to understand the design of building blocks of digital ICs using various modeling techniques.
4. Able to Analyze modes of operation of MOS transistor and its basic electrical properties
5. Able to Calculate the parasitic resistance and capacitance produced by the layouts and thus designing circuits with better performance
6. Design various combinational circuits using gates and transistors for RAM and ROM

**UNIT – I**

INTRODUCTION: Historical Perspective, Issues in Digital Integrated Circuit Design, Quality Metrics of a Digital Design: Cost of an Integrated Circuit, Functionality and Robustness, Performance, Power and Energy Consumption.

**UNIT – II**

MOS TRANSISTOR: The MOS Transistor under Static Conditions, Dynamic Behaviour, The Actual MOS Transistor—Some Secondary Effects, SPICE Models for the MOS Transistor, Method of Logical Effort for transistor sizing.

**UNIT – III**

THE CMOS INVERTER: Introduction, The Static CMOS Inverter — An Intuitive Perspective, Evaluating the Robustness of the CMOS Inverter: The Static Behavior, Switching Threshold, Noise Margins, Robustness Revisited, Performance of CMOS Inverter: The Dynamic Behavior, Computing the Capacitances.

**UNIT – IV**

LOGIC FAMILIES & CHARACTERISTICS: COMS, TTL, ECL, logic families COMS/ TTL, interfacing comparison of logic families.

COMBINATIONAL LOGIC DESIGN USING VHDL: VHDL modeling for decoders, encoders, multiplexers, comparison, adders and subtractors.

**UNIT – V**

SEQUENCIAL IC DESIGN USING VHDL: VHDL modeling for larches, flip flaps, counters, shift registers FSMs. ASM charts.

DIGITAL INTEGRADED SYSTEM BUILDING BLOCKS: Multiplexers and decoders – barrel shifters counters digital single bit adder.

**UNIT – VI**

MEMORIES: ROM Internal structure, 2D decoding commercial type timing and applications, RAM internal structure.

CPLD: XC 9500 series family CPLD architecture – CLB internal architecture, I/O block internal structure.

FPGA: Conceptual of view of FPGA – classification based on CLB internal architecture I/O block architecture.

**TEXT BOOKS:**

1. Analog Integrated circuit Design by David A Johns, Ken Martin, John Wiley & Sons.

2. Analysis and design of Analog Integrated Circuits, by Gray, Hurst Lewis, Meyer. John Wiley &

Sons.

3. Design of Analog CMOS Integrated Circuits, Behzad Razavi, TMH

4. Digital Integrated Circuit Design by Ken Martin, Oxford University 2000

5. Digital Design Principles & Practices” by John F Wakerly, Pearson Education &Xilinx Design

Series, 3rd Ed. (2002)

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – I Sem.**

**EMBEDDED SYSTEMS DESIGN**

**(Common to VLSI and DECS)**

**Subject Code : 16MVL1005 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives:**

1. Understand the general overview of Embedded Systems; distinguish between ES and GPCS, components & major application areas of ES.
2. Learn about Characteristics and Quality attributes of Embedded Systems and core of the embedded system.
3. Gain the ability to make intelligent choices for selection of memory and different communication interfaces.
4. Understand different embedded firmware design approaches and languages.
5. Study the overview of Real Time Operating Systems
6. To clearly differentiate the different issues that arises in real time operating systems.

**Outcomes:**

* 1. Distinguish Embedded System & General Purpose Computing System and formulate the typical embedded system
  2. Describe the characteristics, Quality Attributes of an Embedded System and core of the embedded systems.
  3. Explain the concepts of different types of memory and communication interfaces.
  4. Use firmware approaches and modern engineering tools necessary for developing firmware & hardware in embedded system design
  5. Explain the concepts of Real Time Operating System (RTOS) based embedded system design.
  6. Identify the issues in real time operating systems and choose an appropriate RTOS.

**UNIT -I**:

Introduction to Embedded Systems Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems,

**UNIT -II**:

Characteristics and Quality Attributes of Embedded Systems. Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS),

**UNIT-III:**

Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

**UNIT -IV:**

Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer. Embedded Firmware: Embedded Firmware Design Approaches and Development Languages.

**UNIT -V:**

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

**UNIT -VI:**

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

**TEXT BOOKS:**

1. Introduction to Embedded Systems - Shibu K.V, McGraw Hill.

**REFERENCE BOOKS:**

1. Embedded Systems - Raj Kamal, TMH.

2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.

3. Embedded Systems – Lyla, Pearson, 2013

4. An Embedded Software Primer - David E. Simon, Pearson Education.

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – I Sem.**

**Semiconductor Device Modeling**

**(Common to VLSI and DECS)**

**Subject Code : 16MVL1006 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives:**

1. To understand the impact of semi conductor physics
2. To analyze diode equation, I-V characteristics time dependent and switching characteristics
3. To explain MOS capacitances with respective surface potential, electro static potential,
4. To study bipolar device models for circuit and time dependent analysis.
5. To provide knowledge of long channel and short channel MOSFETS.
6. To study long channel and short channel charge model.

**Outcomes:**

1. Apply the concepts of current density equations, continuity equation
2. Develop consciousness on diode leakage current, excess charge carriers, and diffusion capacitance.
3. Function effectively on poly silicon work function and depletion effects
4. Design solutions with appropriate bipolar device modeling
5. Demonstrate knowledge and understanding of long and short channel MOSFETS.
6. Apply appropriate models to complex engineering activities with an understanding of limitations.

**UNIT -I**:

Physics of Semiconductors Energy bands in solids-carrier Concentration in intrinsic and extrinsic semiconductors, carrier transport in silicon-drift and diffusion current, velocity saturation, basic equations for device operation-poisson’s equation, current-density equations, continuity equation.

**UNIT -II**:

P-N Junctions Built-in potential, diode equation, current-voltage characteristics-temperature dependence and diode leakage currents, time-dependent and switching characteristics: excess charge carriers, diffusion capacitance.

**UNIT -III**

MOS capacitors Surface potential, electrostatic potential and charge distribution in silicon, capacitances in MOS structure-low frequency and high frequency C-V characteristics, polysilicon work function and depletion effects, charge in Si-SiO2 interface, effects of interface traps on device characteristics-surface generation and recombination.

**UNIT -IV**

Bipolar Transistors NPN & PNP transistors, ideal Current-Voltage Characteristics, Bipolar Device Models for Circuit and Time-Dependent Analyses.

**UNIT -V**

MOSFET Devices Long-channel MOSFETs: drain current model, I-V characteristics, sub-threshold characteristics, temperature dependence of threshold voltage, channel mobility. Short Channel MOSFETs: short channel effects, velocity saturation, channel length modulation, source-drain series resistance.

**UNIT -VI**

**Dynamic model:**

Meyer model, charge based capacitance model, long channel charge model, short channel charge model limitations of quasi- static model, small signal model parameters.

**TEXT BOOKS:**

1. Y. Taur, T. H. Ning, “Fundamentals of Modern VLSI Devices”, Cambridge University Press.

2. NarainArora, “MOSFET Modeling for VLSI simulation: Theory and Practice”, World Scientific

publishing Co Pte Ltd.

**REFERENCE BOOKS**

1. S. M. Sze, “Physics of Semiconductor Devices”, John Wiley & Sons”, 3rd Edition.

2. B. G. Streetman, S. Banerjee, “Solid State Electronic Devices”, Prentice Hall India.

3. Tor A. Fjeldly, TrondYtterdal, Michael S. Shur, “Introduction to Device Modeling and Circuit

Simulation”, Wiley Publication.

4. YannisTsividis, “Operation and Modeling of the MOS Transistor”, Oxford University Press.

5. Robbert F. Pierret, “Semiconductor Device Fundamentals”, Addison Wesley Publishers

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – I Sem.**

**HARDWARE & SOFTWARE CO-DESIGN**

**Subject Code : 16MVL1007 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives**

1. Learn basic concepts of Hardware software Co-design
2. Know the Co-design Models, Algorithms and methodology etc…
3. Understand Embedded Architectures, Embedded Software Development needs, Compilation Technologies.
4. Learn the Design specification and verification.
5. Know the System-level performance modeling, low-level performance modeling and High-level synthesis

**Outcomes**

1. Analyze any embedded system’s hardware and software design issues
2. Choose different Co-design Models, Algorithms and methodology etc., for embedded design
3. Apply Embedded Software Development tools, Compilation Techniques for embedded applications
4. Test the hardware and software individually
5. Explain the System-level performance modeling, low-level performance modeling and High-level synthesis

**UNIT I**

CO- DESIGN ISSUES AND CO- SYNTHESIS ALGORITHMS: Co - Design Models, Architectures, Languages, a Generic Co-Design Methodology, Hardware – Software Synthesis Algorithms: Hardware – Software Partitioning, Distributed System Co-Synthesis.

**UNIT II**

PROTOTYPING AND EMULATION: Prototyping and Emulation techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping.

**UNIT III**

TARGET ARCHITECTURES: Architecture Specialization Techniques, System Communication infrastructure, Target Architectures and Application System Classes, Architectures for Control Dominated System and Data – Dominated Systems.

**UNIT IV**

COMPILATION TECHNIQUES AND TOOLS FOR EMBEDDED PROCESSOR ARCHITECTURES: Modern Embedded Architectures, Embedded Software Development needs, Compilation, Technologies, Practical Consideration in a compiler Development Environment.

**UNIT V**

DESIGN SPECIFICATION AND VERIFICATION: Design, Co- Design, The Co- Design Computational Model, Concurrency, coordinating Concurrent Computations, interfacing components, Design Verification, Implementation Verification, Verification Tools, Interface Verification

**UNIT VI**

LANGUAGES FOR SYSTEM – LEVEL SPECIFICATION AND DESIGN: System – Level Specification, Design representation for system level synthesis, System level Specification Languages, Heterogeneous Specifications and Multi Language Co – Simulation. The cosyma system and Lycos system.

**TEXT BOOKS:**

1. Hardware / Software Co – Design Principles and Practice- Jorgen Staunstrup, Wayne Wolf-2009, Springer
2. Hardware / Software Co – Design Principles and Practice, Kluwer Academic Publishers

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – I Sem.**

**EMBEDDED AND REAL TIME SYSTEMS**

**Subject Code : 16MVL1008 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives:**

1. Understand the general overview of Embedded Systems
2. Gain the ability to make differentiate between different processors
3. Learn about different state machine and concurrent process models.
4. Study the overview of various communication processes used in RTOS.
5. Gain the ability to make intelligent choices between different RTOS concepts.
6. Study the overview of different embedded and Real Time Operating Systems

**Outcomes:**

1. Demonstrate the basics of embedded systems
2. Explain the different processors and their technologies.
3. Use the various state machine and concurrent process models of RTOS
4. Extrapolate the different RTOS communication processes
5. Identify the appropriate embedded/RTOS concept
6. Discuss the different operating systems associated with embedded and RTOS.

**UNIT - I**

INTRODUCTION: Embedded systems over view, design challenges, processor technology, Design technology, Trade-offs. Single purpose processors RT-level combinational logic, sequential logic (RT level), custom purpose processor design (RT level), optimizing custom single purpose processors.

**UNIT - II**

GENERAL PURPOSE PROCESSORS: Basic architecture, operations, programmer's view, development environment, Application specific Instruction -Set processors (ASIPs)-Micro controllers and Digital signal processors.

**UNIT - III**

STATE MACHINE AND CONCURRENT PROCESS MODELS: Introduction, models Vs Languages, finite state machines with data path model(FSMD),using state machines, program state machine model(PSM, concurrent process model, concurrent processes, communication among processes, synchronization among processes, Implementation, data flow model, real-time systems.

**UNIT - IV**

COMMUNICATION PROCESSES: Need for communication interfaces, RS232/UART, RS422/RS485, USB, Infrared, IEEE1394Firewire, Ethernet, IEEE 802.11, Blue tooth.

**UNIT - V**

EMBEDDED/RTOS CONCEPTS-I: Architecture of the Kernel, Tasks and task scheduler, interrupt service routines, Semaphores, Mutex.

EMBEDDED/RTOS CONCEPTS-II: Mailboxes, Message Queues, Event Registers, Pipes-Signals.

**UNIT - VI**

EMBEDDED/RTOS CONCEPTS -III: Timers-Memory Management-Priority inversion problem embedded operating systems-Embedded Linux-Real-time operating systems-RT Linux-Handheld operating systems-Windows CE.

**TEXT BOOKS:**

1. Embedded System Design-A Unified Hardware/Software Introduction- Frank Vahid, Tony D.

Givargis, John Wiley & Sons, Inc.2002.

2. Embedded/Real Time Systems- KVKK prased, Dreamtech press-2005.

3. Introduction to Embedded Systems - Raj Kamal, TMS-2002.

**REFERENCE BOOKS:**

1. Embedded Microcomputer Systems-Jonathan W.Valvano,Books/Cole,ThomsonLeaarning.

2. An Embedded Software Primer- David E.Simon, pearson Ed.2000

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – I Sem.**

**HDL PROGRAMMING LABORATORY**

**(Common to M. Tech. VLSI and DECS)**

**Subject Code : 16MVL1101 Internal Marks: 40**

**Credits : 2 External Marks: 60**

**Objectives**

1. Study the Xylinx software.

2. Analyze and experience with principle of designing digital circuits

3. Simulate the digital circuits by using VHDL/Verilog.

4. Synthesize the digital circuits by using VHDL

5. Implement the digital circuits by using VHDL.

**Outcomes**

1. Simulate the digital circuits by using VHDL/ Verilog.

2. Synthesis and implement the digital circuits by using VHDL.

3. Generate RTL schematics and timing constraints.

4. Produce power report and Place and Route report of digital circuit synthesis.

5. Implement the digital circuits by using FPGA devices

**The students are required to simulate, synthesize and implement the following experimental part, on the VHDL/Verilog environment.**

1. Digital Circuits Description using Verilog and VHDL

2. Verification of the Functionality of Designed circuits using function Simulator.

3. Timing simulation for critical path time calculation.

4. Synthesis of Digital circuits

5. Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.

6. Implementation of Designed Digital Circuits using FPGA and CPLD devices.

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – II Sem.**

**Mixed Signal IC design**

**Subject Code : 16MVL1009 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives**

1. To introduce circuit design concepts for basic building blocks used in mixed signal integrated circuit designs.
2. To provide students with the skills to design mixed‐signal integrated circuits with these building blocks.

**Outcomes**

At the end of the course the student will be able to

1. Learn analysis of switched capacitor circuits.
2. Learn non ideal effects in switched capacitor circuits.
3. Know dynamics of PLL blocks.
4. Demonstrate the fundamentals of data converters.
5. Compare different data converters.
6. Learn over sampling converters.

**UNIT -I:**

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits - basic building blocks, Operation and Analysis.

**UNIT –II:**

Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, bi-quad filters.

**UNIT -III:**

Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs-Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non-ideal effects in PLLs-PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications

**UNIT -IV:**

Data Converter Fundamentals: DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters

**UNIT -V:**

Nyquist Rate A/D Converters: Successive approximation converters, Flash converter, Two-step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time-interleaved converters.

**UNIT -VI:**

Oversampling Converters: Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multibit quantizers, Delta sigma D/A

**TEXT BOOKS:**

1. Design of Analog CMOS Integrated Circuits- Behzad Razavi, TMH Edition, 2002

2. CMOS Analog Circuit Design - Philip E. Allen and Douglas R. Holberg, Oxford University Press,

International Second Edition/Indian Edition, 2010.

3. Analog Integrated Circuit Design- David A. Johns, Ken Martin, Wiley Student Edition, 2013

**REFERENCE BOOKS:**

1. CMOS Integrated Analog-to- Digital and Digital-to-Analog converters-Rudy Van De Plassche,

Kluwer Academic Publishers, 2003

2. Understanding Delta-Sigma Data converters-Richard Schreier, Wiley Interscience, 2005.

3. CMOS Mixed-Signal Circuit Design - R. Jacob Baker, Wiley Interscience, 2009.

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – II Sem.**

**ALGORITHMS FOR VLSI DESIGN AUTOMATION**

**Subject Code : 16MVL1010 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives:**

The main objective of this course is to

1. Explain the various algorithms used to design VLSI in automation.
2. Illustrate the various optimization techniques in the process of automation.
3. Describe various floor planning methods for layout design.
4. Describe various Routing techniques for layout design.
5. Discuss various MCM and FPGA technologies

.

**Outcomes:**

Student will be able to

1. Explain VLSI Design Flow, design automachine tools and algorithms
2. Examine various Routing algorithms for layout design.
3. Apply various Routing algorithms for layout design.
4. Explain logic synthesis and verification
5. Apply various Routing algorithms for FPGA.
6. Apply various Routing algorithms for MCM.

**UNIT – I**

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational Complexity, Tractable and Intractable Problems.

**UNIT – II**

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

**UNIT – III**

Layout Compaction, Placement, Floor planning and Routing Problems, Concepts and Algorithms MODELING AND SIMULATION: Gate Level Modeling and Simulation, Switch level Modeling and simulation.

**UNIT – IV**

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary –Decision diagram, Two – Level Logic Synthesis.

HIGH LEVEL SYNTHESIS: Hardware Models, Internal representation of the input algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High – level Transformations.

**UNIT – V**

PHYSICAL DESIGN AUTOMATION OF FPGA’S: FPGA technologies, Physical Design cycle for FPGA’s partitioning and routing for segmented and staggered models.

**UNIT – VI**

PHYSICAL DESIGN AUTOMATION OF MCM’S: MCM technologies, MCM physical design cycle, Partitioning, Placement – Chip array based and full custom approaches, Routing – Maze routing, Multiple stage routing, Topologic routing, Integrated Pin – Distribution and routing, routing and programmable MCM’s

**TEXT BOOKS:**

1. Algorithms for VLSI Design Automation, S.H.Gerez, WILEY student edition, Johnwiley& Sons

(Asia) Pvt. Ltd, 1999.

2. Algorithms for VLSI Physical Design Automation, 3rd edition, Naveed Sherwani, Springer

International Edition, 2005

**REFERENCE BOOKS:**

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, Wiley, 1993

2. Modern VLSI Design: Systems on silicon – Wavne Wolf, Pearson Education Asia, 2nd Edition,

1998

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – II Sem.**

**LOW POWER VLSI DESIGN**

**Subject Code : 16MVL1011 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives**

1. To familiarize with the different types of Low power design methods/models used in VLSI design.
2. To study the concepts on different levels of power estimation and optimization techniques.
3. Introduce the technology, design concepts, electrical properties and modelling of Very Large Scale Integrated circuits.
4. Identify sources of power in an IC and suitable techniques to reduce the power dissipation in ICs
5. Design of CMOS low power IC, approaches for power consumption estimation and methods of reducing switching & leakage power.

**Outcomes**

Student will be able to

1. Describe in detail the need and use of low power devices in the design of VLSI.
2. Design chips used for battery-powered systems and high-performance circuits not exceeding power limits.
3. Apply in practice technology-level, circuit-level, and system-level power optimization techniques.
4. Design a significant VLSI design project having set of objective criteria and design constraints.
5. Design the conventional CMOS and BICOMS circuits using logic gates.
6. Analyze the quality measures and design perspectives of latches and Flip-Flaps.

**UNIT – I**

LOW POWER DESIGN AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

MOS/BiCMOS PROCESSES: Realization of Bi CMOS processes: Low cost-medium speed digital, High performance-High cost digital, Analog/Digital Integrated BiCMOS.

**UNIT – II**

ISOLATION IN BiCMOS: Isolation in BiCMOS, Isolation Techniques in MOS - LOCOS, Shallow and Deep Trench, Advanced Isolation techniques - Dielectric Isolation (DI), Wafer bonding, Smart cut process.

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes - Key process steps , SOI CMOS, lateral BJT on SOI, Future trends and directions of CMOS/BiCMOS processes.

**UNIT – III**

DEVICE MODELING: MOSFET Spice Models, Advanced MOSFET models, limitations of MOSFET models, Bipolar models - Ebers Moll model, Gummel poon model, HICUM model

**UNIT – IV**

Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment

**UNIT – V**

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and BiCMOS logic gates, Performance Evaluation.

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Operation, Performance and comparative Evaluation of Advanced BiCMOS Digital circuits - Full-Swing Multi drain/Multi collector CBiCMOS, Quasi-CBiCMOS, Feedback type BiCMOS, ESD-free Bi CMOS.

**UNIT – VI**

LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

**TEXT BOOKS:**

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl (3 Authors)- Pearson Education Asia 1st Indian reprint,2002

**REFERENCE BOOKS:**

1. Digital Integrated circuits, J.Rabaey PH. N.J 1996

2. CMOS Digital ICs sung-moKang and yusufleblebici 3rd edition TMH2003 (chapter 11)

3. VLSI DSP systems, Parhi, John Wiley & sons, 2003 (chapter 17)

4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International

Conferences and Symposia.

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – II Sem.**

**DESIGN OF FAULT TOLERANT SYSTEMS**

**Subject Code : 16MVL1012 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives:**

1. Design systems to achieve goals like dependability, reliability, availability, safety, performability, maintainability, and testability
2. Explain about fault tolerant systems
3. Understand self checking circuits
4. Understand fail safe design
5. Analyze testability for combinational and sequential circuits
6. Describe LFSR and BIST concepts

**Outcomes:**

1. Calculate dependability, reliability, availability, safety, performability, maintainability, and testability
2. Analyze redundancy systems
3. Design circuits that generate test patterns
4. Describe fail safe design circuits.
5. Develop the combinational and sequential circuits for testability
6. Summarize the LFSR and built in self test concepts

**UNIT – I**

BASIC CONCEPTS: Reliability concepts, Failure & Faults, Reliability and failure rate, Relation between reliability and meantime between failure, Maintainability and Availability, Reliability of series, Parallel and Parallel-Series combinational circuits.

**UNIT – II**

FAULT TOLERANT DESIGN: Basic concepts – Static, dynamic, hybrid, Triple Modular Redundant System, Self purging redundancy, Siftout redundancy (SMR), SMR Configuration, Use of error correcting code, Time redundancy and software redundancy.

**UNIT – III**

SELF CHECKING CIRCUITS: Basic concepts of Self checking circuits, Design of Totally Self Checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.

**UNIT – IV**

FAIL SAFE DESIGN: Strongly fault secure circuits, fail-safe design of sequential circuits using partition theory and Berger code, totally self-checking PLA design.

**UNIT – V**

DESIGN FOR TESTABILITY FOR COMBINATIONAL AND SEQUENTIAL CIRCUITS: Basic concepts of testability, controllability and observability, the Reed Muller’s expansion technique, OR-AND-OR design, use of control and syndrome testable design. Level Sensitive Scan Design (LSSD).

**UNIT – VI**

Theory and operation of LFSR, LFSR as Signature analyzer, Multiple-input Signature Register. BUILT IN SELF TEST: BIST concepts, Test pattern generation for BIST exhaustive testing, pseudorandom testing, pseudo exhaustive testing, constant weight patterns.

**TEXT BOOKS:**

1. Parag K. Lala – “Fault Tolerant & Fault Testable Hardware Design” (PHI)

2. M. Abramovili, M.A. Breues, A. D. Friedman – “Digital Systems Testing and Testable Design”

Jaico publications.

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – II Sem.**

**VLSI SIGNAL PROCESSING**

**(Common to M. Tech. VLSI and DECS)**

**Subject Code : 16MVL1013 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives:**

1. Understand the pipelining and parallel processing techniques to the VLSI system
2. Analyze the retiming, unfolding & folding concepts for register minimization
3. Understand the systolic architectures
4. Understand the various arithmetic circuits for signal processing
5. Understand and apply the fast convolution algorithms for signal processing applications
6. Explain different low power algorithms.
7. Explain redundant number representation and numerical strength reduction algorithms.

**Outcomes:**

1. Design parallel processors in VLSI systems
2. Implement the register minimization using the retiming, unfolding & folding concepts.
3. Design systolic architecture using canonical mapping and generalized mapping.
4. Analyze the fast convolution algorithms and use them for signal processing applications
5. Design low power multipliers using bit level arithmetic circuits.
6. Design low power multipliers using multiple constant algorithms.

**UNIT – I**

Introduction to DSP :Introduction, Typical DSP algorithms, Representation of DSP algorithms , Iteration Bound-Data flow graph Representation, loop bound, iteration bound, algorithms for computing iteration bound, iteration bound of multirate dataflow graphs. Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power,

**UNIT – II:**

RETIMING: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNFOLDING: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

Folding: Introduction - Folding Transform – Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems

**UNIT – III:**

Systolic Architecture Design: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain delays.

**UNIT – IV:**

Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

**A**LGORITHM STRENGTH REDUCTION FILTERS AND TRANSFORMS: Introduction, parallel FIR filters, Discrete cosine Transform and Inverse DCT

**UNIT – V:**

BIT-LEVEL ARITHMETIC ARCHITECTURES-Introduction, parallel multipliers, Interleaved floor plan and Bit plane based digital filters, Bit-Serial Multipliers, Bit-Serial filter design and implementation, Canonic Signed Digit Arithmetic, Distributed Arithmetic

**UNIT – VI:**

REDUNDANT ARITHMETIC: Introduction, Redundant number representation, Carry free Radix-2 Addition and Subtraction, Hybrid Radix-4 addition, Radix -2 Hybrid redundant multiplication architectures, data format conversion, redundant to non redundant converter

NUMERICAL SRENGTH REDUCTION: Introduction, Sub expression Elimination, Multiple constant multiplications, Sub expression sharing in digital filters, additive and multiplicative number splitting.

**TEXT BOOKS:**

1. Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation –1998,

Wiley Inter Science.

2. Kung S. Y, H. J. While House, T. Kailath, VLSI and Modern Signal processing, 1985, Prentice

Hall.

**REFERENCE BOOKS**:

1. Jose E. France, Yannis Tsividis, Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing –1994, Prentice Hall.
2. Medisetti V. K, VLSI Digital Signal Processing, IEEE Press (NY), USA, 1995.

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – II Sem.**

**SYSTEM MODELLING & SIMULATION**

**(Common to M. Tech. VLSI and DECS)**

**Subject Code : 16MVL1014 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives**

1. Analyze approaches to system modeling and simulation
2. Design simulation model for linear systems.
3. Develop simulation for motion control models.
4. Analyze state machine model
5. Develop Petri nets for a problem and its analysis
6. Analyze the simulation of queuing systems and optimization.

**Outcomes**

1. Analyze the given system or problem
2. Design a model to represent the system or problem
3. Develop simulation models for time and event driven systems
4. Analyze State machine models
5. Design simulation models for given system using petri nets
6. Analyze the queuing systems and optimization

**UNIT – I**

BASIC SIMULATION MODELING: Systems, Models and Simulation, Discrete Event Simulation, Simulation of Single server queuing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

**UNIT – II**

SIMULATION SOFTWARE: Comparison of simulation packages with Programming Languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

**UNIT – III**

BUILDING SIMULATION MODELS: Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

MODELING TIME DRIVEN SYSTEMS: Modeling input signals, delays, System Integration, Linear Systems, Motion Control models, numerical experimentation.

**UNIT – IV**

EXOGENOUS SIGNALS AND EVENTS: Disturbance signals, state machines, petri nets & analysis, System encapsulation.

MARKOV PROCESS: Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous –Time Markov processes.

**UNIT – V**

EVENT DRIVEN MODELS: Simulation diagrams, Queuing theory, simulating queuing systems, Types of Queues, Multiple Servers.

**UNIT – VI**

SYSTEM OPTIMIZATION: System identification, Searches, Alpha/beta trackers, multidimensional optimization, modeling and simulation methodology.

**TEXT BOOKS:**

1. System Modeling & Simulation, An introduction – Frank L. Severance, John Wiley & Sons, 2001.

2. Simulation Modeling and Analysis – Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

**REFERENCE BOOK:**

1. Systems Simulation – Geoffery Gordon, PHI, 1978.

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – II Sem.**

**CPLD AND FPGA ARCHITECTURE AND APPLICATIONS**

**Subject Code : 16MVL1015 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives**

1. Understand the features, architectures & applications of CPLD and FPGA devices.
2. To study the designing methods of CPLD and FPGA devices.

**Outcomes**

At the end of the course, the student will be able to:

1. List the features and know the architecture of different PLDs
2. Design the different families of CPLD & FPGs
3. Realize out finite state machines
4. Understand the concept system level design by using design methods

**UNIT –I**

PROGRAMMABLE LOGIC DEVICES: ROM, PLA, PAL, CPLD, FPGA – Features, Architectures, Programming, Applications and Implementation of MSI circuits using Programmable logic Devices.

**UNIT – II**

CPLDs: Complex Programmable Logic Devices, Altera series – Max 5000/7000 series and Altera FLEX logic-10000 series CPLD, AMD’s- CPLD (Mach 1 to 5), Cypress FLASH 370 Device technology, Lattice pLSI’s architectures – 3000 series – Speed performance and in system programmability.

**UNIT – III**

FPGAs: Field Programmable Gate Arrays- Logic blocks, routing architecture, design flow, technology mapping for FPGAs, Case studies Xilinx XC4000 & ALTERA’s FLEX 8000/10000, FPGAs: AT &T ORCA’s

**UNIT – IV**

FINITE STATE MACHINES (FSM): Top Down Design, State Transition Table, State assignments for FPGAs, Realization of state machine charts using PAL, Alternative realization for state machine charts using microprogramming, linked state machine, encoded state machine.

FSM ARCHITECTURES: Architectures Centered around non registered PLDs, Design of state machines centered around shift registers, One Hot state machine, Petrinets for state machines-Basic concepts and properties, Finite State Machine-Case study.

**UNIT – V**

DESIGN METHODS: One –hot design method, Use of ASMs in one-hot design method, Applications of one hot design method, Extended Petri-nets for parallel controllers, Meta Stability, Synchronization, Complex design using shift registers.

**UNIT – VI**

SYSTEM LEVEL DESIGN: Controller, data path designing, Functional partition, Digital front end digital design tools for FPGAs & ASICs, System level design using mentor graphics EDA tool(FPGA Advantage), Design flow using CPLDs and FPGAs.

CASE STUDIES: Design considerations using CPLDs and FPGAs of parallel adder cell, parallel adder sequential circuits, counters, multiplexers, parallel controllers.

**TEXT BOOKS:**

1. Field Programmable Gate Array Technology - S. Trimberger, Edr, 1994, Kluwer Academic Publications.

2. Engineering Digital Design - RICHARD F.TINDER, 2nd Edition, Academic press.

3. Fundamentals of logic design-Charles H. Roth, 4th Edition Jaico Publishing House.

**REFERENCES BOOKS:**

1. Digital Design Using Field Programmable Gate Array, P.K.Chan& S. Mourad,1994, Prentice Hall.

2. Field programmable gate array, S. Brown, R.J.Francis, J.Rose ,Z.G.Vranesic, 2007,BSP.

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – II Sem.**

**System on Chip (SOC) Design**

**Subject Code : 16MVL1016 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives**:

The student will be able to

1. Understand the components of system, hardware and software.
2. Know the basic concepts of processor architecture and instructions.
3. Describe external and internal memory of SOC.
4. Get knowledge of bus models of SOC
5. Explain SOC design approach.

**Outcomes**:

At the end of the course the student will be able to

1. Memorize the system architecture, components of system hardware and software.
2. Know the basic concepts of processor architecture and instructions and delays.
3. Describe external and internal memory of SOC and organization.
4. Explain bus architectures and models of SOC.
5. Know SOC customization and reconfiguration technologies.
6. Apply the knowledge of SOC design in real time applications

**UNIT –I:**

**Introduction to the System Approach**: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, An approach for SOC Design, System Architecture and Complexity

**UNIT –II:**

**Processors:** Introduction , Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

**UNIT –III:**

**Memory Design for SOC**: Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time, Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

**UNIT -IV:**

**Interconnect** : Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time.

**UNIT –V:**

**SOC Customization**: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping design onto Reconfigurable devices, Instance- Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Parallelism.

**UNIT –VI**:

**Application Studies / Case Studies**: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

**TEXT BOOKS**:

1. Computer System Design System-on-Chip - Michael J. Flynn and Wayne Luk, Wiely India Pvt.

Ltd.

2. ARM System on Chip Architecture – Steve Furber –2 nd Ed., 2000, Addison Wesley Professional.

**REFERENCE BOOKS**:

1. Design of System on a Chip: Devices and Components – Ricardo Reis, 1st Ed., 2004, Springer

2. Co-Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology) – Jason Andrews – Newnes, BK and CDROM.

3. System on Chip Verification – Methodologies and Techniques –Prakash Rashinkar, Peter Paterson and Leena Singh L, 2001, Kluwer Academic Publishers.

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**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (VLSI System Design) – II Sem.**

**MIXED SIGNAL SIMULATION LABORATORY**

**Subject Code : 16MVL1102 Internal Marks: 40**

**Credits : 2 External Marks: 60**

**Objectives**

* + 1. Study the Microwind and PSPICE software’s.
    2. Summarize the layout design rules
    3. Design layouts for various combinational logic circuits and logic functions.
    4. Examine Parasitic Values from Layout.
    5. Learn industrial techniques for mixed signal IC test, which include dc measurement, frequency response, harmonic and inter modulation distortion, and noise behavior

**Outcomes**

1. Design layouts for various combinational logic circuits and logic functions.
2. Examine mixed signal design flow
3. Design Analog Circuits Simulation using Spice Software
4. Analyze Layout Extraction for Analog & Mixed Signal Circuit.
5. Measure frequency response, harmonic and inter modulation distortion, and noise behavior

**By considering suitable complexity Mixed-Signal application based circuits (circuits consisting of both analog and digital parts), the students are required to perform the following aspects using necessary software tools:**

1. Analog Circuits Simulation using Spice Software.

2. Digital Circuits Simulation using Xilinx Software.

3. Mixed Signal Simulation Using Mixed Signal Simulators.

4. Layout Extraction for Analog & Mixed Signal Circuits.

5. Parasitic Values Estimation from Layout.

6. Layout Vs Schematic.

7. Net List Extraction.

8. Design Rule Checks.