LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
1	4/1/16	Introduction	1	chalk & dust		
2	6/1/16	Discrete time signals				
3	7/1/16	Linear shift invariant	1	"		
4	8/1/16	systems				
5	11/1/16	stability and	1	"		
6	18/1/16	Causality				
7	20/1/16	Linear constant	1	"		
8	21/1/16	coefficient diffegn				
9	22/1/16	freq domain	1	"		
10	25/1/16	representation of				
11	27/1/16	Discrete Fourier	1	"		
12	28/1/16	Series — properties				
13	29/1/16	of DFS, DFT	1	"		
14	1/2/16	representation periodic				
15	3/2/16	Discrete Fourier Transform	1	"		
16	4/2/16	properties DFT,	2	"		
17	5/2/16	linear convolution				
18	8/2/16	sequences using DFT,	2	"		
19	10/2/16	Computation of DFT				
20	11/2/16	Fast fourier Transform	2	"		
21	12/2/16	Radix 2 Decimation in Time				
22	15/2/16	DIF Algorithm	2	"		
23	16/2/16	Inverse FFT				
24	22/2/16	Z Transform,	2	"		
25	24/2/16	Definition				
26	25/2/16	Properties Roc	2	"		
27	26/2/16	Inverse Z Transform				
28	29/2/16	Relation b/w fourier Transform & Z Transform	2	"		
29	2/3/16	Solution for LCCDE Block diagram representation	3	"		
30	3/3/16	of LCCDE. Basic structure of IIR systems	3	"		
31	4/3/16	Direct form cascade parallel form structures	3	"		
32	7/3/16	Analog filter approximation Butterworth filter design	3	"		
33	9/3/16	chebyshev filter design	3	"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
34	10/3/16	Design IIR filter digital from analog filter	3	chalk & dust		
35	11/2/16	Mapping differentials, & linear transformation	3	"		
36	14/3/16	Bilinear transform method	3	"		
37	16/3/16	Matched Z transform	3	"		
38	17/3/16	Design examples	3	"		
39	18/3/16	Frequency transformation	3	"		
40 41	21/3/16 24/3/16	Problem on IIR filter	3	"		
42	31/3/16	FIR digital filters introduction	4	"		
43	1/4/16	Basic structure of FIR system	4	"		
44	4/4/16	Direct form cascade	4	"		
45	6/4/16	Frequency sample lattice	4	"		
46	7/4/16	Characteristics of FIR digital filter	4	"		
47	8/4/16	Frequency response	4	"		
48	13/4/16	Design FIR digital filter using window	4	"		
47	14/4/16	Frequency sampling technique	4	"		
50	18/4/16	Comparison IIR & FIR filters	4	"		
51	20/4/16	Multirate signal processing	4	"		
52	21/4/16	Decimation, interpolation	4	"		
53	22/4/16	Sampling rate conversion	4	"		
54	25/4/16	Implementation of sampling rate conversion	4	"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review	Period	(Te
54	25/4/16	Introduction to DSP processor	5	chalk & dust				
		Introduction to programmable DSP	5	"			59	9
55	27/4/16	multiplier and Accumulator (MAC)	5	"				
		Modified Buy structures	5	"			60	4
		memory access Scheme in DSP	5	"				
56	28/4/16	multiple access memory	5	"				
		multiport memory	5	"				
57	29/4/16	VLSI architecture	5	"				
		pipelining	5	"				
57	30/4/16	Special addressing modes	5	"				
		onchip peripherals	5	"				
		Architecture of TMS320C5x	5	"				
58	2/5/16	Introduction	5	"				
		bus structure	5	"				
		central Arithmetic Logic unit	5	"				
58	2/5/16	Auxillary registers	5	"				
		Index Registers	5	"				
		Auxillary registers	5	"				
59	3/5/16	Block move Address registers	5	"				
		Parallel Logic unit	5	"				

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
		plenty mapped registery	5	chalk & dust		
59	8/5/16	program controller	5	u		
		functions in the study registers	5	v		
60	9/5/16	architr registory	5	v		
		archit peripherals	5	u		failer