LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective A Upon Rev
		UNIT-I				
1	22/8	OP-AMP: General Consideration- Block, 2 stage OP-AMPS	I	BB		
2	23/8	Gain, Loosing stage Comparison D/P Rank	"	"		
3	26/8	limitations, Slew Rate Current mirrors	"	"		
4	29/8	Single Stage Amplifier- Intro	"	PPT		
5	30/8	Simple CMOS, BJT current mirrors	"	"		
6	1/9	Cascode wilson wilder current mirr	"	"		
7	2/9	Noise: Types of noise Thermal noise	"	"		
8	6/9	Flicker noise, Noise in op-Amps	"	"		
9	8/9	UNIT- II PLL- Introduction	II	"		
10	9/9	PLL Concepts	"	"		
11	13/9	The PLL in locked Condition.	"	"		
12	15/9	Integrated ckt PLL's	"	"		
13	16/9	Phase detector XOR	"	"		
14	19/9					
15	20/9	Case-Study	"	"		
		Analysis of	"	"		
16	22/9	the 560 B	"	"		
		Monolithic	"	"		
17	23/9	PLL.		"		

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
18	26/9	UNIT III Switched Capacitor circuits - Intro	III	BB		
19	27/9	Basic building blocks of opAmps	"	PPT		
20	29/9	Capacitors, switches.	"	BB		
21	30/9	Non-over lapping clocks.	"	PPT		
		Basic operations & Analysis				
22	3/10	Resistor equivalents of a Switched Capacitor	"	PPT		
23	4/10	Parasitic sensitive Integrator	"	PPT		
24	6/10	Parasitic Insensitive Integrators	"	BB		
25	13/10	Signal flow graph Analysis	"	"		
	2/10					
26	14/10		"	PPT		
		17/10 — 22/10 — I mid				

LESSON PLAN

Period	Date (Tentative)	Topic UNIT I-IV	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
27	24/10	logic families & characteristics	IV	PPT		
28	25/10	CMOS, TTL,	"	"		
29	27/10	ECL, logic families CMOS, TTL,	"	"		
30	28/10	Interfacing	"	"		
		comparision of logic				
31	31/10	families.	"	BB		
32	1/11	combinational logic designs using VHDL:	"	BB		
33	3/11	VHDL modeling for Decoders.	"	PPT		
34	4/11	Encoders	"	"		
35	7/11	multiplexers.	"	BB		
36	8/11	Sequential		"		

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
37	10/11	Sequential IC design using VHDL.	II	BB		
38	11/11	VHDL modeling for Latches.	II	BB		
39	15/11	Flipflops, Counters.	II	PPT		
40	17/11	Shift Registers.	II	BB		
		UNIT-5	V			
41	18/11	Digital Integrated system building blocks: multiplexers	II	PPT		
42	21/11	Decoders.	I	BB		
43	22/11	Barrel Shifters.	I	PPT		
44	24/11	Counters. Digital	II	BB		
		Single bit adders				
45	25/11	Memories: ROM	II	PPT		
		Internal Structure				
46	28/11	2D-decoding	II	BB		
		Commercial type timing & ASMs.				

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
47	29/11	RAm Internal structure.	II	II		
		UNIT-VI	VI			
48	1/12	Comparator: using an op-amp & a	II	II		
		Comparator - charge injection error -				
49	2/12	Latched Comparator	II	PPT		
50	5/12	Nyquist Rate D/A Converter: Decoder	II	BB		
		based converter,				
51	6/12	Resistor String Converter, folded	II	PPT		
		resistor.				
52	8/12	String Converter Binary Scale	II	II		
		converter.				
53	9/12	Binary weighted resistor	II	II		
		converters.				
54	12/12	Nyquist Rate A/D Converter:	II	II		
		Integrating Converters.				
55	13/12	Successive approximation	II	II		
		Converters.				
56	15/12	DAC based Successive	II	II		
57	16/12	Approximation	II	II		

19/12/16 — 24/12/16 — 2 MID