LESSON PLAN

Branch: I M.Tech **Semester**: I **Subject** : DSD&T

Acadamic year: 2016-17 **faculty :Swathi jallu**

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action upon Review
		Design of Digital Systems	I			
1.	22.08.2016	Introduction	I	Black Board		
2.	23.08.2016	ASM charts example for ASM chart	I	B.B		
3.	26.08.2016	Data path design	I	B.B		
4.	29.08.2016	Control Logic implementation,	I	B.B		
5.	30.08.2016	Reduction of state tables- Row matching method	I	B.B		
6.	01.09.2016	State equivalence finding by implication chart method	I	B.B		
7.	02.09.2016	Equivqlent sequential circuits	I	B.B		
8.	06.09.2016	Incompletely specified state tables				
9.	08.09.2016	Equivalent State assignments.	I	B.B		
10.	09.09.2016	Guide lines for State assignments.	I	B.B		
		Sequential circuit design	II			
11.	13.09.2016	Introduction		B.B		
12.	16.09.2016	Design of Iterative circuits	II	B.B		
13.	19.09.2016	Design of a Comparator	II	B.B		
14.	20.09.2016	Design of sequential circuit by using ROM	II	B.B		
15.	23.09.2016	Design of sequential circuit by using PLA	II	B.B		
16.	26.09.2016	Introduction to CPLD & FPGA	II	B.B		
17.	27.09.2016	Design of sequential circuit by using CPLD	II	B.B		
18.	29.09.2016	Design of sequential circuit by using FPGA	II	B.B		
		Fault modelling	III			
19.	30.09.2016	Introduction	III	B.B		
20.	03.10.2016	Fault classes and models	III	B.B		
21.	04.10.2016	Stuck at faults, bridging faults	III	B.B		
22.	14.10.2016	Transition and Intermittent faults.	III	B.B		
23.	14.10.2016	Test generation& Fault diagnosis	III	B.B		

24.	18.10.2016	of Combinational circuits by conventional methods	III	B.B		
25.	19.10.2016	Path Sensitization technique,	III	B.B		
26.	20.10.2016	Example for finding stuck-at faults	III	B.B		
27.	21.10.2016	Boolean difference method,	III	B.B		
28.	24.10.2016	Kohavi algorithm.	III	B.B		
		Test pattern generation	IV			
29.	25.10.2016	D – algorithm	IV	B.B		
30.	26.10.2016	PODEM	IV	B.B		
31.	27.10.2016	Random testing	IV	B.B		
32.	28.10.2016	Transition count testing,	IV	B.B		
33.	31.10.2016	Signature analysis and testing for bridging faults	IV	B.B		
34.	01.11.2016	**fault Diagnosis in sequential circuits:**	IV	B.B		
35.	03.11.2016	State identification,	IV	B.B		
36.	04.11.2016	Machine identification	IV	B.B		
37.	07.11.2016	fault detection experiment	IV	B.B		
		PLA	V			
38.	08.11.2016	Introduction to PLA	V	B.B		
39.	10.11.2016	Design using PLA's,	V	B.B		
40.	11.11.2016	PLA minimization	V	B.B		
41.	14.11.2016	PLA folding.	V	B.B		
42.	15.11.2016	PLA Maximum	V	B.B		
43.	17.11.2016	optimum folding:	V	B.B		
44.	18.11.2016	PLA TESTING,		B.B		
45.	21.11.2016	Fault models	V	B.B		
46.	22.11.2016	Test generation	V	B.B		
47	24.11.2016	Testable PLA design.	V	B.B		
		Asynchronous Sequential Machine				
48	25.11.2016	Introduction	VI	B.B		
49	28.11.2016	Fundamental mode model	VI	B.B		
50	29.11.2016	Flow table	VI	B.B		
51	01.12.2016	State reduction in the	VI	B.B		
52	02.12.2016	Flow table	VI	B.B		
53	05.12.2016	Minimal closed covers,	VI	B.B		
54	06.12.2016	Races in the asynchronous sequential machines	VI	B.B		
55	08.12.2016	Cycles in the asynchronous sequential machines.	VI	B.B		

56	09.12.2016	Hazards and cycles in the	VI	B.B		
57	12.12.2016	State machines	VI	B.B		
58	13.12.2016	Prime Implication table	VI	B.B		

CR: CLASS ROOM **PPT: POWER POINT PRESENTATION** **LCD**

TEXT BOOKS :

1. Digital Design Principles & Practices – John F. Wakerly, PHI/ Pearson Education Asia, 2005, 3/e.
2. Digital IC Applications – Atul P.Godse and Deepali A.Godse, Technical Publications, Pune, 2005.
3. VHDL Primer – J. Bhasker, PHI,3rd Edition.

Reference books:

1. Digital System Design Using VHDL – Charles H. Roth Jr., PWS Publications,1998.
2. Digital Logic and Computer Design by Morris Mano, Prentice Hall.

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