LESSON PLAN

[illegible]	Date [illegible]	Topic	Unit No	Teaching Methodology	Remarks
[illegible]	[illegible]	[illegible] structure	6	Black board & PPT	
[illegible]	[illegible]	Data flow Descrip tion	6	"	
[illegible]	[illegible]	Test Bench for the [illegible] CPU	6	"	
[illegible]	[illegible]	[illegible] Realistic [illegible]	6	"	
[illegible]	[illegible]	Structure, [illegible] & Modeling	6	"	
[illegible]	[illegible]	[illegible] modeling language	6	"	

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Faculty Sign
51	[illegible]	User defined attributes	4	Black Board & PPT		
52	[illegible]	Packing Basic utilities	4	"		
		UNIT-5 DATA FLOW DESCRIPTION IN VHDL		"		
53	[illegible]	Multiplexing and Data Selection	5	"		
54	[illegible]	State Machine Description	5	"		
55	[illegible]	Open collector gates	5	"		
56	[illegible]	Three state Bussing	5	"		
57	[illegible]	A general Data Flow Circuit	5	"		
58	[illegible]	Updating Basic utilities	5	"		
59	[illegible]	Behavioural Description of hardware	5	"		
60	[illegible]	Process statement as action statements	5	"		
61	[illegible]	Sequential wait statements	5	"		
62	[illegible]	Formatted ASCII I/O operation, MSI Based Design	5	"		
		UNIT-6 CPU MODELLING FOR				
		DESCRIPTION IN VHDL				
63	[illegible]	Parwan CPU	6	"		
	[illegible]	Behavioural description of Parwan	6	"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
17	[illegible]	Wiring Interactive Networks	2	Black Board, PPT		
18	[illegible]	Modelling a Test Bench	2	-		
19	[illegible]	Binding Alternative Top Down Wiring	2	-		
				-		
		UNIT - 3 DESIGN ORGANISATIONS & PARAMETERISATIONS - I		-		
20	[illegible]	Definition and	3	-		
21	[illegible]	Usage of Subprograms	3	-		
22	[illegible]	Packaging parts and utilities	3	-		
23	[illegible]	Design Parameterization	3	-		
24	[illegible]	Design Configuration	3	-		
25	[illegible]	Design Libraries	3	-		
		UNIT - 4 DESIGN ORGANISATIONS & PARAMETERISATIONS - II		-		
26	[illegible]	Utilities for high level Description	4	-		
		Type Declarations & Usage	4	-		
27	[illegible]	VHDL Operators	4	-		
28	[illegible]	Subprogram Parameter types & Overloading	4	-		
		Other types	4	-		
29	[illegible]	Type related issues	4	-		
30	[illegible]	Pre defined Attributes	4	-		

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
		UNIT - 1 INTRODUCTION		Black Board, PPT		
1	17/11/15	An overview of Design Procedures used for	1	"		
		System Design using CAD tools	1	"		
2	18/11/15	Design Entry	1	"		
3	19/11/15	Synthesis, Simulation	1	"		
4	21/11/15	Optimization, Place & Route	1	"		
5	24/11/15	Design verification tools	1	"		
6	25/11/15	Examples using commercial PC based on VHDL	1	"		
7	26/11/15	Elements of VHDL	1	"		
8	28/11/15	Top Down Design with VHDL Subprograms	1	"		
9	01/12/15	VHDL Controller Description	1	"		
10	02/12/15	VHDL Operators	1	"		
		UNIT-2 BASIC CONCEPT IN VHDL		"		
11	04/12/15	Characterizing hardware languages	2	"		
12	05/12/15	objects and classes	2	"		
13	08/12/15	Signal Assignments	2	"		
14	09/12/15	Concurrent & sequential Assignments	2	"		
15	10/12/15	Structural specification of hardware parts	2	"		
16	15/12/15	Library wiring of Primitives	2	"		