LESSON PLAN

Subject Code & Name: VLSI TD

Branch: VLSI   **Class / Semester: IM.Tech-SEM 1**   **Academic Year:2014-15**
Faculty: J.Swathi

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective action upon review
		REVIEW OF MICROELECTRONICS & INTRODUCTION	**I**			
1	17.11.2014	Introduction		BB		
2	18.11.2014	Technology trends and projections		BB		
3	19.11.2014	Lithography,oxidation,diffusion metallisation		BB		
4	21.11.2014	Fabrication process of PMOS and NMOS		BB		
5	24.11.2014	Fabrication process of CMOS and BiCMOS		BB		
6	25.11.2014	Basic electrical properties of MOS circuits Ids vs Vds relationship		BB		
7	26.11.2014	MOS,CMOS,BICMOS Inverters,Pass tr		BB		
8	28.11.2014	Zpu/Zpd ratios both 4:1 & 8:1		BB		
9	01.12.2014	latchup in CMOS circuits		BB		
		LAYOUT DESIGN AND TOOLS	**II**			
10	02.12.2014	Introduction, Transistor structures, wires and vias		BB		
11	03.12.2014	Scalable design rules, lambda based design rules, stick diagrams		BB		
12	05.12.2014	Layout diagrams		BB		
13	08.12.2014	Logic gates: static complementary gates		BB		
14	09.12.2014	Delay analysis ,power optimization		BB		
15	10.12.2014	Switch logic, alternative gate circuits		BB		
16	12.12.2014	Low power gates		BB		
17	15.12.2014	RLC tx lines ,interconnect delays		BB		
		COMBINATIONAL LOGIC NETWORKS	**III**			
18	16.12.2014	Introduction, std. cell		BB		
19	17.12.2014	Structure, left edge algorithm		BB		
20	19.12.2014	Simulation, network delay		BB		
21	22.12.2014	Interconnect design				
22	23.12.2014	Power optimization & analysis				
23	24.12.2014	Switch logic networks		BB		
24	26.12.2014	Gate and network testing		BB		

25	29.12.2014	Combinational logic testing		BB		
		SEQUENTIAL LOGIC NETWORKS	IV			
26	30.12.2014	Introduction		BB		
27	31.12.2014	Memory cells and arrays		BB		
28	02.01.2015	Clocking disciplines		BB		
29	19.01.2015	System design of sequential circuits		BB		
30	20.01.2015	Power optimization & analysis		BB		
31	21.01.2015	Design and validation		BB		
32	23.01.2015	Testing of sequential machines		BB		
		FLOORPLANNING	V			
33	26.01.2015	Floor planning introduction		BB		
34	27.01.2015	Floor planning methods		BB		
35	28.01.2015	Off-chip connections				
36	30.01.2015	High level synthesis		BB		
37	02.02.2015	Architecture for low power SOCs		BB		
38	03.02.2015	CPUs				
39	04.02.2015	Embedded CPUs		BB		
40	06.02.2015	Architecture testing		BB		
41	09.02.2015	Validation		BB		
		INTRODUCTION TO CAD SYSTEMS AND CHIP DESIGN	VI			
42	10.02.2015	Introduction		BB		
43	11.02.2015	Chip design		BB		
44	13.02.2015	Layout synthesis		BB		
45	17.02.2015	Layout analysis		BB		
46	18.02.2015	Scheduling and printing		BB		
47	20.02.2015	Hardware/Software Co-design		BB		
48	23.02.2015	Chip-Design methodologies		BB		
49	24.02.2015	Chip-design IBM-ASIC Example		BB		
50	25.02.2015	Kitchen-Timer Chip		BB		
	26.02.2015	Design of Kitchen -Timer chip		BB		

CR: CLASS ROOM   **PPT: POWER POINT PRESENTATION**   **LCD**

Text books:
1. Essentials of VLSI circuits and systems – Kamran Eshraghian, Eshraghian Dougles and A. Pucknell, PHI, 2005.
2. Principles of CMOS VLSI Design – Weste and Eshraghian, Pearson Education, 1999.

Reference books:
1. VLSI Design – Debaprasad Das, Oxford university press, 2010.
2. VLSI Design – A.Albert Raj and T.Latha, PHI Learing private limited 2010.
3. ASIC design - Smith.

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