

# LESSON PLAN

Period	Date (tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action / Upgr. Review
1	12/11/14	Design of Digital Systems Introduction	I			
2	18/11/14	ASM charts				
3	19/11/14	problem solving				
4	21/11/14	Hardware				
5	24/11/14	description <del>language</del>				
6	25/11/14	control sequence method				
7	26/11/14	Reduction of state tables				
8	28/11/14	state Assignment				
9	1/12/14	Sequential circuit II	II			
10	2/12/14	Design Introduction				
11	3/12/14	Design of Identifiable circuits				
12	5/12/14	Design of sequential				
13	8/12/14	data storage ROM, DRAM				
14	9/12/14	sequential circuit				

17	12/12/14	Fault Modeling	III		
18	15/12/14	Fault classes		"	
19	18/12/14	Fault models		"	
20	19/12/14	Stuck-at faults		"	
21	19/12/14	bridging faults		"	
		Transition and		"	
22	22/12/14	Intermittent faults		"	
23	23/12/14	Fault Diagnosis		"	
		in sea-ckts		"	
24	29/12/14	state identification		"	
25	26/12/14	Fault detection exp.		"	
26	29/12/14	Machine Identification		"	
27	30/12/14	Design of fault		"	
28	31/12/14	detection experiment		"	
29	2/1/15	TEST GENERATION	IV	"	
30	10/1/15	Fault diagnosis of		"	
31	20/1/15	combinational ckts by		"	
		conventional methods		"	
32	21/1/15	path Sensitization techniques		"	

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
33	27/1/15	Barlow Difference Method				
34	28/1/15	Kobayashi algorithm		"		
35	30/1/15	TAT Pattern Generation		"		
		D-algorithm		"		
36	2/2/15	PODEM		"		
		Random testing		"		
37	3/2/15	Transition Count Testing		"		
38	4/2/15	Signature analysis		"		
		and testing for		"		
39	6/2/15	bridging faults		"		
40	9/2/15	Programming logic	V	"		
		Arrays		"		
41	10/2/15	Design using PLA's		"		
42	13/2/15	PLA minimization		"		
43	12/2/15	PLA folding		"		
		PLA testing		"		
44	12/2/15	Fault models		"		

