LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
		UNIT-I				
1	17/11	OP-AMPS	I	Black Board		
		one-stage op-Amps				
		Two-Stage op-Amps				
2	18/11	gain boosting stage	I	"		
		Comparison i/p Range, Slew Rate.				
3.	19/11	Simple CMOS, BJT Current Mirror.	I	"		
4.	21/11	Cascade Wilson Widlar Current Mirrors	I	"		
5.	24/11	Common Source Amplifier Source-follower.	I	"		
6.	25/11	Common gate Amplifier.	I	"		
7.	26/11	Bypass or Noise Thermal Noise Flicker Noise.	I	"		
8.	28/11	Noise in op-Amps. Noise in Common Source stage Noise Band width	I	"		
9	1/12	UNIT-II PLL Design.	II	"		
		PLL Concepts, The PLL in the locked Condition of PLL				
10	2/12	Phase Detector.	II	"		
11	3/12	Voltage Controlled Oscillator.	II	"		
12	5/12	Case study: Analysis of The 560B Monolithic PLL	II	"		
13	8/12	UNIT-III SWITCHED CAPACITOR CKTS	III	"		
		Basic Building Blocks op-Amps Capacitors Switches.				
14	9/12	Non overlapping clocks Basic operations and Analysis.	III	"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
		Resistor equivalent to Switched Capacitor.		Black Board		
15	10/12	Parasitic Sensitive Integrator.	III	"		
		Parasitic Insensitive Integrators				
16	10/12	Signal Flowgraph Analysis.	III	"		
		First order Filters.				
17	12/12	Switch Sharing Fully Diff Filters.	III	"		
		Charged Injections				
18	15/12	Switched Capacitor gain Circuits Non Inverting	III	"		
		Capacitor Circuit.				
19	16/12	Precise table gain Circuit.	III	"		
		Other Switched Capacitor Circuits				
20	17/12	Full wave Rectifier	III	"		
		Peak Detector. Sinusoidal Oscillator				
21	19/12	UNIT-IV LOGIC FAMILIES & CHARACTERISTICS	IV	PPT		
		CMOS, TTL, ECL logic families.				
22	22/12	TTL/CMOS Interfacing	IV	"		
23	23/12	Comparison of logic families	IV	BB		
24	29/12	VHDL Modeling for Decoders, encoders.	IV	"		
25	30/12	Multiplexers, Comparators logic families	IV	"		

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Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
26	2/1	Comparators, Adders Subtractors.	IV	Black Board		
27	19/1	VHDL Modeling for Latches.	IV	"		
28	20/1	Flip.Flops, Counters	IV	"		
29	21/1	Shift Registers. FSMS.	IV	"		
30	23/1	ASM Charts.	IV	"		
		UNIT-V				
31	27/1	DIGITAL INTIMATIO SYSTEM BUILDING BLOCKS Multiplexers, and decoders.	V	"		
32	28/1	Binary Adders Counters digital Single bit Adders.	V	"		
33	30/1	MEMORIES: ROM Internal Structure	V	"		
34	2/2	RD decoding Combined type linking and Applications.	V	"		
35	3/2	RAM Internal Structure.	V	"		
36	4/2	CPLD: XC9500 Series family CPLD architecture	V	PPT		
37	6/2	CLB Internal Architecture.	V	"		
38	9/2	I/O Block Internal Architecture.	V	"		
		UNIT-VI				
39	10/2	COMPARATORS: using OP-Amp for a Comparator	VI	Black Board		
40	11/2	Change projection errors.	VI	"		
41	13/2	Latched Comparator	VI	"		

LESSON PLAN

Period	Date (Tentative)	Topic	Unit No.	Teaching Methodology	Remarks	Corrective Action Upon Review
42	16/2	NYQUIST RATE D/A CONVERTERS:	VI	Black Board		
43	17/2	Decoder Based Converter.	VI	"		
44	18/2	Resistor String Converters.	VI	"		
45	19/2	Folded Resistor String Converter	VI	"		
46	20/2	Binary Scaled Converters.	VI	"		
47	23/2	Binary Weighted Resistor Converters.	VI	"		
48	24/2	Reduced Resistance Ratio ladders.	VI	"		
49	25/2	R-2R Based Converters.	VI	"		
50	26/2	Thermometer Code Current mode D/A	VI	"		
51	27/2	NYQUIST RATE A/D Converters.	VI	"		
52	27/2	Integrating Converts.	VI	"		
53	27/2	DAC Based SAR.	VI	"		
54	27/2	FLASH Converters	VI	"		
55	27/2	Time Interleaved A/D Converters.	VI	"		