**COURSE STRUCTUREAND SYLLABI**

**FOR**

**M.TECH**

**DIGITAL ELECTRONICS AND COMMUNICATION SYSTEMS**

**From The Academic Year 2016 – 2017**

****

**ADITYA Institute of Technology And Management**

***(An Autonomous Institution)***

**Approved by AICTE, Permanently Affiliated to JNTUK, Kakinada**

**Accredited by NBA & NAAC, Recognized by UGC under 2(f) & 12(b)**

**K. Kotturu, TEKKALI – 532 201, Srikakulam Dist., A.P.,**

**ADITYA INSTITUTE OF TECHNOLOGY AND MANAGEMENT, TEKKALI**

***(An Autonomous Institution)***

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**COURSE STRUCTURE (AR16)**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **M. Tech. (DECS) – 1st SEMESTER** | | | | | | | | |
| **S. No.** | **SUBJECT**  **CODE** | **SUBJECT** | **L** | **P** | **C** | **MARKS** | | |
| **INT** | **EXT** | **TOTAL** |
| 1 | 16MVL1001 | Digital System Design& Testing | 4 | - | 4 | 40 | 60 | 100 |
| 2 | 16MVL1002 | Digital Design Through HDL | 4 | - | 4 | 40 | 60 | 100 |
| 3 | 16MDE1001 | Digital Data Communications | 4 | - | 4 | 40 | 60 | 100 |
| 4 | 16MDE1002 | Analog and Digital IC Design | 4 | - | 4 | 40 | 60 | 100 |
| 5 |  | ***Elective – I*** |  |  |  |  |  |  |
| 16MVL1005 | a) Embedded System Design | 4 | - | 4 | 40 | 60 | 100 |
| 16MVL1006 | b) Semiconductor Device Modeling |
| 6 |  | ***Elective – II*** |  |  |  |  |  |  |
| 16MDE1003 | a) Advanced Signal Processing | 4 | - | 4 | 40 | 60 | 100 |
| 16MDE1004 | b) Radar Signal Processing |
| 7 | 16MVL1101 | HDL Programming Laboratory | - | 4 | 2 | 40 | 60 | 100 |
|  | | TOTAL | 24 | 4 | 26 | 280 | 420 | 700 |

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **M. Tech. (DECS) – 2nd SEMESTER** | | | | | | | | |
| **S. No.** | **SUBJECT**  **CODE** | **SUBJECT** | **L** | **P** | **C** | **MARKS** | | |
| **INT** | **EXT** | **TOTAL** |
| 1 | 16MDE1005 | Spread Spectrum Communications | 4 | - | 4 | 40 | 60 | 100 |
| 2 | 16MDE1006 | Detection and Estimation of Signals | 4 | - | 4 | 40 | 60 | 100 |
| 3 | 16MDE1007 | Wireless Communication & Networks | 4 | - | 4 | 40 | 60 | 100 |
| 4 | 16MDE1008 | Coding Theory and Techniques | 4 | - | 4 | 40 | 60 | 100 |
| 5 |  | ***Elective – III*** |  |  |  |  |  |  |
| 16MVL1013 | a) VLSI Signal Processing | 4 | - | 4 | 40 | 60 | 100 |
| 16MVL1014 | b) System Modeling and Simulation |
| 6 |  | ***Elective – IV*** |  |  |  |  |  |  |
| 16MDE1009 | a) Adaptive Signal Processing | 4 | - | 4 | 40 | 60 | 100 |
| 16MDE1010 | b) Software Defined Radio |
| 7 | 16MDE1101 | Advanced Communication Laboratory | - | 4 | 2 | 40 | 60 | 100 |
|  | | TOTAL | 24 | 4 | 26 | 280 | 420 | 700 |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **M. Tech. (DECS) – 3rd SEMESTER** | | | | | | | |
| **S. No.** | **SUBJECT**  **CODE** | **SUBJECT** | **L** | **P** | **C** | **Marks** | |
| **I** | **E** |
| 1 | 16MDE2201 | Technical Seminar | - | - | 2 | 100 | - |
| 2 | 16MDE2202 | Project Work | - | - | 12 | - | - |
| TOTAL | | | - | | 14 | 100 | |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **M. Tech. (DECS) – 4th SEMESTER** | | | | | | | |
| **S. No.** | **SUBJECT**  **CODE** | **SUBJECT** | **L** | **P** | **C** | **Marks** | |
| **I** | **E** |
| 1 | 16MDE2203 | Project Work | - | - | 14 | - | - |
| TOTAL | | | - | | 14 |  | |

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – I Sem.**

**DIGITAL SYSTEM DESIGN & TESTING**

**(Common to M. Tech. VLSI and DECS)**

**Subject Code : 16MVL1001 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives**

The main objective of this course is to

1. Explain the designing principles of various digital systems
2. Analyze a given digital system and decompose it into logical blocks involving both combinational and sequential circuit elements.
3. Explain Reduction of state tables and state assignments.
4. Describe the Fault Modeling and Test pattern Generation methods.
5. Describe PLA minimization and testing.

**Outcomes**

Student will be able to

1. Apply knowledge of digital systems, Sequential Circuit Design and design of digital logic circuits
2. Explain fault modeling and classes.
3. Apply knowledge of different algorithms for generating test patterns.
4. Detect states and faults in sequential circuits.
5. Explain PLA minimization and testing.
6. Analyze an asynchronous sequential machines

**UNIT – I**

DESIGN OF DIGITAL SYSTEMS: ASM charts, Data path design and Control Logic implementation, Reduction of state tables, State assignments.

**UNIT – II**

SEQUENTIAL CIRCUIT DESIGN: Design of Iterative circuits, Design of sequential circuits using ROMs and PLAs, Sequential circuit design using CPLD, FPGAs.

**UNIT – III**

FAULT MODELING: Fault classes and models – Stuck at faults, bridging faults, transition and intermittent faults.

TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

**UNIT – IV**

TEST PATTERN GENERATION: D – algorithm, PODEM, Random testing, transition count testing, Signature analysis and testing for bridging faults.

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: State identification, Machine identification, and fault detection experiment.

**UNIT – V**

PROGRAMMING LOGIC ARRAYS: Design using PLA’s, PLA minimization and PLA folding.

PLA TESTING: Fault models, Test generation and Testable PLA design.

**UNIT – VI**

ASYNCHRONOUS SEQUENTIAL MACHINE: fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

**TEXT BOOKS:**

1. Z. Kohavi – “Switching & finite Automata Theory” (TMH).

2. N. N. Biswas – “Logic Design Theory” (PHI).

3. Nolman Balabanian, Bradley Calson – “Digital Logic Design Principles” – Wily Student Edition

2004.

**REFRENCE BOOKS:**

1. M. Abramovici, M. A. Breues, A. D. Friedman – “Digital System Testing and Testable Design”,

Jaico Publications.

2. Charles H. Roth Jr. – “Fundamentals of Logic Design”.

3. Frederick. J. Hill & Peterson – “Computer Aided Logic Design” – Wiley 4th Edition.

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – I Sem.**

**DIGITAL DESIGN THROUGH HDL**

**(Common to M. Tech. VLSI and DECS)**

**Subject Code : 16MVL1002 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives**

1. Learn the design and implement of the fundamental digital logic circuits using Verilog hardware description language.
2. Find the design issues of system on chip.
3. Write the Verilog & VHDL Programming for combinational and sequential circuits using different styles of modeling.
4. Design large Systems using tasks and functions.
5. Design large systems using packages and libraries.

**Outcomes**

1. Design and implement the fundamental digital logic circuits using Verilog & VHDL at various levels of abstractions.
2. Write the Test bench simulation programs for all logic circuits.
3. Use the tasks and functions in digital system design process.
4. Design a large digital systems based on small modules.
5. Analyze the timing parameters of simulation and synthesis process.

**UNIT I:**

INTRODUCTION TO VERILOG : ASIC Design flow, FPGA Design flow, comparison between ASIC Design flow and FPGA Design flow, Features of Verilog HDL, different Levels of Design Description, Simulation, Test bench Simulation and Synthesis process,

LANGUAGE ELEMENTS OF VERILOG HDL: Introduction, Keywords, Identifiers, White Space Characters, Comments, Numbers, Strings, Logic Values, Strengths, Data Types, Scalars and Vectors, Parameters, Memory, Operators, System Tasks, Exercises.

**UNIT II:**

GATE LEVEL MODELING : Introduction, AND Gate Primitive, Module Structure, Other Gate Primitives, Illustrative Examples, Tri-State Gates, Array of Instances of Primitives, Additional Examples, Design of Flip flops with Gate Primitives, Delays, Strengths and Contention Resolution, Net Types, Design of Basic Circuits, Exercises.

**UNIT III:**

BEHAVIORAL MODELING : Introduction, Operations and Assignments, Functional Bifurcation, Initial Construct, Always Construct, Examples, Assignments with Delays, Wait construct, Multiple Always Blocks, Designs at Behavioral Level, Blocking and Non blocking Assignments, The case statement, Simulation Flow. iƒ and iƒ-else constructs, assign-deassign construct, repeat construct, for loop, the disable construct, while loop, forever loop, parallel blocks, force-release construct, Event.

**UNIT IV:**

MODELING AT DATA FLOW LEVEL: Introduction, Continuous Assignment Structures, Delays and Continuous Assignments, Assignment to Vectors, Operators. Verilog HDL programming for different combinational and sequential circuits.

SYSTEM TASKS, FUNCTIONS, AND COMPILER DIRECTIVES : Introduction, Parameters, Path Delays, Module Parameters, System Tasks and Functions, File-Based Tasks and Functions, Compiler Directives, Hierarchical Access, General Observations, Exercises, Function, Tasks, FSM Design (Moore and Mealy Machines)

**UNIT V:**

INTRODUCTIONTO VHDL: BASIC LANGUAGE ELEMENTS: Identifiers, Data Objects, Data Types, Operators.

BEHAVIORAL MODELING: Entity Declaration, Architecture Body, Process Statement, Variable Assignment Statement, Signal Assignment Statement, Wait Statement, If Statement, Case Statement, Null Statement, Loop Statement.

DATAFLOW MODELING: Concurrent Signal Assignment Statement, Concurrent versus Sequential Signal Assignment, Conditional Signal Assignment Statement.

**UNIT VI:**

STRUCTURAL MODELING: Component Declaration, Component Instantiation, Examples, Resolving Signal Values.

GENERICS AND CONFIGURATIONS: Generics, Configuration Specification, Configuration Declaration.

PACKAGES AND LIBRARIES: Package Declaration, Package Body, Design Libraries, Design File.

**Text Books:**

1. Design through Verilog HDL – T.R. Padmanabhan and B. Bala Tripura Sundari, WSE, 2004

IEEEP press.

2. A Verilog Primer – J. Bhaskar, BSP, 2003.

3. A VHDL Primer - J. Bhaskar, PHI, 3rd edition

**Reference Books:**

1. Fundamentals of Logic Design with Verilog – Stephen. Brown and Zvonko Vranesic, TMH, 2005.

2. Digital Systems Design using VHDL – Charles H Roth, Jr. Thomson Publications, 2004.

3. Advanced Digital Design with Verilog HDL – Michael D. Ciletti, PHI, 2005.

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – I Sem.**

**DIGITAL DATA COMMUNICATIONS**

**Subject Code : 16MDE1001 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives:**

1. Know the basics of the communications, and how the data is communicated in terms of digital modulation techniques.
2. Understand data transmission modes.
3. Explain Data Communication Protocols.
4. Discuss how to use the digital transmission rather than analog and also multiplexing techniques like TDM, FDM, and WDM.
5. Explain the various wireless local area network architectures and different multimedia systems.

**Outcomes:**

Students will be able to

1. Describe various digital modulation techniques and calculate probability of error and bit error rate
2. Compare and contrast the data transmission modes: serial and parallel as well as synchronous, asynchronous, and isochronous with relevant examples.
3. Describe Data Communication Protocols.
4. Demonstrate wireless communication systems and also work with satellite communication systems using different multiplexing techniques like TDM, FDM and WDM.
5. Explain various wireless local area network architectures the application services like wireless LAN and Bluetooth.
6. Illustrate the multimedia services.

**UNIT – I**

DIGITAL MODULATION TECHNIQUES: FSK, MSK, BPSK, QPSK, 8-PSK, 16-PSK, 8- QAM, 16 - QAM, Band width efficiency carrier recovery DPSK, clock recovery, Probability of error and bit error rate.

**UNIT – II**

DATA COMMUNICATIONS: Serial, Parallel configuration, Topology, Transmission modes, Error Control Synchronization, LCU.

**UNIT – III**

Serial and Parallel Interfaces, Telephone Networks and Circuits and data modems, Data Communication Protocols, Character and block Mode, Asynchronous and Synchronous Protocols, Public Data Networks, ISDN.

**UNIT – IV**

DIGITAL MULTIPLEXING: TDM, T1 carrier, CCITT, CODECS, COMBO CHIPS, Line Encoding, T-carrier, Frame Synchronization Inter Leaving, Statistical TDM. FDM, Hierarchy, Wave Division Multiplexing.

**UNIT – V**

LOCAL AREA NETWORKS: Token ring, Ethernet, Traditional, Fast and GIGA bit Ethernet, FDDI. WIRELESS LANS IEEE 802.11: Architecture Layers, Addressing, Blue Tooth Architecture Layers, L2 Cap, Other Upper Layers.

**UNIT – VI**

MULTI MEDIA: Digitalizing Video and Audio Compression Streaming Stored and Live Video and Audio, Real Time Interactive Video and Audio.

**TEXT BOOKS:**

1. Advanced Electronic Communication Systems - W. Tomasi, 5 ed., 2008, PEI.
2. Data Communication and Computer Networking - B. A.Forouzan, 3rd ed., 2008, TMH.

**REFERENCES:**

1. Data and Computer Communications - William Stallings, 8th ed., 2007, PHI.

2. Data Communication and Tele Processing Systems - T. Housely, 2nd Edition, 2008, BSP.

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – I Sem.**

**ANALOG AND DIGITAL IC DESIGN**

**Subject Code : 16MDE1002 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives**

1. To provide theoretical basics for analysis and design of analog integrated circuits.
2. To understand various current mirror configurations in application to different amplifiers.
3. To introduce PLL concept in integrated circuits.
4. To introduce Nyquist data converters useful in many applications.
5. Comprehend the different issues related to the development of digital Integrated circuits including fabrication, circuit design, implementation Methodologies, testing, design methodologies and tools and future Trends.
6. Understanding the main principles of various Digital building blocks used in IC design.

**Outcomes**

**At the end of the course the student will be:**

1. Design two stage CMOS operational amplifiers and compensation techniques.
2. Illustrate current mirror circuits in single stage CMOS operational amplifiers.
3. Illustrate advanced current mirrors and comparators.
4. Understand PLL use in integrated circuits
5. Understand switched capacitor circuits.
6. Design and analyze CMOS A/D and D/A data converters of different types.

**UNIT – I**

OPERATIONAL AMPLIFIERS: General considerations one – stage op-amps, two stage op-amps-gains boosting stage- comparison I/P range limitations slew rate.

CURRENT MIRRORS AND SINGLE STAGE AMPLIFIERS: simple COMS, BJT current mirror, Cascade Wilson Wilder current mirrors.

NOISE: Types of Noise – Thermal Noise-flicker noise- Noise in op amps

**UNIT – II**

PHASED LOCKED LOOP DESIGN: PLL concepts- The phase locked loop in the locked condition Integrated circuit PLLs – phase Detector- Voltage controlled oscillator case study: Analysis of the 560 B Monolithic PLL.

**UNIT – III**

SWITHCHED CAPACITORS CIRCUITS: Basic Building blocks op-amps capacitors switches – non-over lapping clocks- Basic operations and analysis-resistor equivalence of la switched capacitor parasitic sensitive integrator parasitic insensitive integrators signal flow graph analysis

**UNIT – IV**

LOGIC FAMILIES & CHARACTURISTICS: COMS, TTL, ECL, logic families COMS/ TTL, interfacing comparison of logic families.

COMBINATIONAL LOGIC DESIGN USING VHDL: VHDL modeling for decoders, encoders, multiplexers,

SEQUENCIAL IC DESIGN USING VHDL: VHDL modeling for larches, flip flaps, counters, shift registers

**UNIT – V**

DIGITAL INTEGRADED SYSTEM BUILDING BLOCKS: Multiplexers and decoders – barrel shifters counters digital single bit adder.

MEMORIES: ROM Internal structure, 2D decoding commercial type timing and applications, RAM internal structure.

**UNIT – VI**

COMPARATORS: Using an op-amp for a comparator-charge injection error- latched comparator.

NYQUIST RATE D/A CONVERTERS: Decoder based converter resistor storing converters folded resister string converter – Binary scale converters – Binary weighted resistor converters

NYQUIST RATE A/D CONVERTERS: Integrating converters – successive approximation converters.DAC based successive approximation

**TEXT BOOKS:**

1. Analog Integrated circuit Design by David A Johns, Ken Martin, John Wiley & Sons.

2. Analysis and design of Analog Integrated Circuits, by Gray, Hurst Lewis, Meyer. John Wiley

& Sons.

3. Design of Analog CMOS Integrated Circuits, Behzad Razavi, TMH

4. Digital Integrated Circuit Design by Ken Martin, Oxford University 2000

5. Digital Design Principles & Practices” by John F Wakerly, Pearson Education & Xilinx Design

Series, 3rd Ed.(2002)

**REFERENCE BOOKS:**

1. Ken Martin, Digital Integrated Circuit Design Oxford University,2000.

2. John F Wakerly, “Digital Design Principles & Practices”, Pearson Education & Xilinx Design

Series, 3rd Ed.(2002)

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – I Sem.**

**EMBEDDED SYSTEMS DESIGN**

**(Common to VLSI and DECS)**

**Subject Code : 16MVL1005 Internal Marks : 40**

**Credits : 4 External Marks: 60**

**Objectives:**

1. Understand the general overview of Embedded Systems; distinguish between ES and GPCS, components & major application areas of ES.
2. Learn about Characteristics and Quality attributes of Embedded Systems and core of the embedded system.
3. Gain the ability to make intelligent choices for selection of memory and different communication interfaces.
4. Understand different embedded firmware design approaches and languages.
5. Study the overview of Real Time Operating Systems
6. To clearly differentiate the different issues that arises in real time operating systems.

**Outcomes:**

* 1. Distinguish Embedded System & General Purpose Computing System and formulate the typical embedded system
  2. Describe the characteristics, Quality Attributes of an Embedded System and core of the embedded systems.
  3. Explain the concepts of different types of memory and communication interfaces.
  4. Use firmware approaches and modern engineering tools necessary for developing firmware & hardware in embedded system design
  5. Explain the concepts of Real Time Operating System (RTOS) based embedded system design.
  6. Identify the issues in real time operating systems and choose an appropriate RTOS.

**UNIT -I**:

Introduction to Embedded Systems Definition of Embedded System, Embedded Systems Vs General Computing Systems, History of Embedded Systems, Classification, Major Application Areas, Purpose of Embedded Systems,

**UNIT -II**:

Characteristics and Quality Attributes of Embedded Systems. Typical Embedded System: Core of the Embedded System: General Purpose and Domain Specific Processors, ASICs, PLDs, Commercial Off-The-Shelf Components (COTS),

**UNIT-III:**

Memory: ROM, RAM, Memory according to the type of Interface, Memory Shadowing, Memory selection for Embedded Systems, Sensors and Actuators, Communication Interface: Onboard and External Communication Interfaces.

**UNIT -IV:**

Reset Circuit, Brown-out Protection Circuit, Oscillator Unit, Real Time Clock, Watchdog Timer. Embedded Firmware: Embedded Firmware Design Approaches and Development Languages.

**UNIT -V:**

RTOS Based Embedded System Design: Operating System Basics, Types of Operating Systems, Tasks, Process and Threads, Multiprocessing and Multitasking, Task Scheduling.

**UNIT -VI:**

Task Communication: Shared Memory, Message Passing, Remote Procedure Call and Sockets, Task Synchronization: Task Communication/Synchronization Issues, Task Synchronization Techniques, Device Drivers, How to Choose an RTOS.

**TEXT BOOKS:**

1. Introduction to Embedded Systems - Shibu K.V, McGraw Hill.

**REFERENCE BOOKS:**

1. Embedded Systems - Raj Kamal, TMH.

2. Embedded System Design - Frank Vahid, Tony Givargis, John Wiley.

3. Embedded Systems – Lyla, Pearson, 2013

4. An Embedded Software Primer - David E. Simon, Pearson Education.

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – I Sem.**

**Semiconductor Device Modeling**

**(Common to VLSI and DECS)**

**Subject Code : 16MVL1006 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives:**

1. To understand the impact of semi conductor physics
2. To analyze diode equation, I-V characteristics time dependent and switching characteristics
3. To explain MOS capacitances with respective surface potential, electro static potential,
4. To study bipolar device models for circuit and time dependent analysis.
5. To provide knowledge of long channel and short channel MOSFETS.
6. To study long channel and short channel charge model.

**Outcomes:**

1. Apply the concepts of current density equations, continuity equation
2. Develop consciousness on diode leakage current, excess charge carriers, and diffusion capacitance.
3. Function effectively on poly silicon work function and depletion effects
4. Design solutions with appropriate bipolar device modeling
5. Demonstrate knowledge and understanding of long and short channel MOSFETS.
6. Apply appropriate models to complex engineering activities with an understanding of limitations.

**UNIT -I**:

Physics of Semiconductors Energy bands in solids-carrier Concentration in intrinsic and extrinsic semiconductors, carrier transport in silicon-drift and diffusion current, velocity saturation, basic equations for device operation-poisson’s equation, current-density equations, continuity equation.

**UNIT -II**:

P-N Junctions Built-in potential, diode equation, current-voltage characteristics-temperature dependence and diode leakage currents, time-dependent and switching characteristics: excess charge carriers, diffusion capacitance.

**UNIT -III**

MOS capacitors Surface potential, electrostatic potential and charge distribution in silicon, capacitances in MOS structure-low frequency and high frequency C-V characteristics, polysilicon work function and depletion effects, charge in Si-SiO2 interface, effects of interface traps on device characteristics-surface generation and recombination.

**UNIT -IV**

Bipolar Transistors NPN & PNP transistors, ideal Current-Voltage Characteristics, Bipolar Device Models for Circuit and Time-Dependent Analyses.

**UNIT -V**

MOSFET Devices Long-channel MOSFETs: drain current model, I-V characteristics, sub-threshold characteristics, temperature dependence of threshold voltage, channel mobility. Short Channel MOSFETs: short channel effects, velocity saturation, channel length modulation, source-drain series resistance.

**UNIT -VI**

**Dynamic model:**

Meyer model, charge based capacitance model, long channel charge model, short channel charge model limitations of quasi- static model, small signal model parameters.

**TEXT BOOKS:**

1. Y. Taur, T. H. Ning, “Fundamentals of Modern VLSI Devices”, Cambridge University Press.

2. NarainArora, “MOSFET Modeling for VLSI simulation: Theory and Practice”, World Scientific

publishing Co Pte Ltd.

**REFERENCE BOOKS**

1. S. M. Sze, “Physics of Semiconductor Devices”, John Wiley & Sons”, 3rd Edition.

2. B. G. Streetman, S. Banerjee, “Solid State Electronic Devices”, Prentice Hall India.

3. Tor A. Fjeldly, TrondYtterdal, Michael S. Shur, “Introduction to Device Modeling and Circuit

Simulation”, Wiley Publication.

4. YannisTsividis, “Operation and Modeling of the MOS Transistor”, Oxford University Press.

5. Robbert F. Pierret, “Semiconductor Device Fundamentals”, Addison Wesley Publishers

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – I Sem.**

**ADVANCED SIGNAL PROCESSING**

**Subject Code : 16MDE1003 Internal Marks : 40**

**Credits : 4 External Marks: 60**

**Objectives:**

1 To have an overview of DFT & FFT Transforms.

2 To study the design of IIR filters.

3 To study the design of FIR filters.

~~4~~ To illustrate the structures of FIR system

5 To understand the power spectral estimation

6 To analyze finite word length effects on DSP systems

**Outcomes:**

At the end of the course, the student will be able to:

1 Comprehend the DFTs and FFTs.

2 Design IIR filters

3 Design FIR filters

4 Analyze the structures of FIR system

5 Analyze the power spectrum estimation

6 Comprehend the Finite word length effects in Fixed point DSP Systems

**UNIT – I**

DISCRETE FOURIER TRANSFORMS: Properties of DFT, Linear Filtering methods based on the DFT, Overlap-save, Overlap -Add methods, frequency analysis of signals. Radix-2 FFT and Split- Radix FFT algorithms The Goertzel and Chirp Z transform algorithms.

**UNIT – II**

DESIGN OF IIR FILTERS: Design of IIR filters using Butterworth & Chebyshev approximations, frequency transformation techniques, structures for IIR systems –cascade, parallel, lattice & lattice-ladder structures.

**UNIT – III**

DESIGN OF FIR FILTERS: Fourier series method, Windowing techniques, design of digital filters based on least – squares method, pade approximations, least squares design, wiener filter methods.

**UNIT – IV**

STRUCTURES FOR FIR SYSTEMS: cascade, parallel, lattice & lattice-ladder structures.

**UNIT – V**

POWER SPECTRAL ESTIMATION: Estimation of spectra from finite duration observation of signals, Nonparametric methods: Bartlett, Welch & Blackmann & Tukey methods. Relation between auto correlation & model parameters, Yule - Waker & Burg Methods, MA & ARMA models for power spectrum estimation.

**UNIT – VI**

ANALYSIS OF FINITE WORD LENGTH EFFECTS IN FIXED-POINT DSP SYSTEMS: Fixed, Floating Point Arhimetic – ADC quantization noise & signal quality – Finite word length effect in IIR digital Filters – Finite word-length effects in FFT algorithms.

**TEXTBOOKS:**

1. Digital Signal Processing –Principles, Algorithms Applications by J.G.Proakis & D.G.Manolokis,

PHI.

2. DSP – A Pratical Approach – Emmanuel C.Ifeacher Barrie. W. Jervis, Pearson Education.

**REFERENCE BOOK:**

1. Discrete Time signal processing - Alan V Oppenheim & Ronald W Schaffer, PHI.

2. Modern spectral Estimation techniques by S. M .Kay, PHI, 1997

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – I Sem.**

**RADAR SIGNAL PROCESSING**

**Subject Code : 16MDE1004 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives:**

1. To understand the fundamental issues involved in radar signal processing and about matched filter.
2. To learn about different signal models used in Radar signal processing for target detection.
3. To learn about Pulsed radar signals**.**
4. To learn about different pulse compression techniques.
5. To understand function of Doppler radar and target detection fundamentals.
6. To learn phase coding techniques for the enhancement of radar performance.

**Outcomes:**

After completion of the course, the student will be able to

1. Revisit analysis of radar fundamentals and design matched filters in noise environment.
2. Analyzevarious signal models for radars
3. Perform modelling with various parameter configurations can be efficiently achieved.
4. Comprehend types of pulse compression techniques for increasing range resolution.
5. Analyze statistical Framework necessary for the development of automatic target detection.
6. Comprehend different phase coding techniques for various radars.

**UNIT - I**

RANGE EQUATION & MATCHED FILTER: Radar Range Equation, Radar Detection with Noise Jamming, Beacon and Repeater Equations, Bi - static Radar Matched filter Receiver – Impulse Response, Frequency Response Characteristic and its Derivation, Matched Filter and Correlation Function, Correlation Detection and Cross - Correlation Receiver. Efficiency of Non - Matched Filters, Matched Filter for Non - White Noise.

**UNIT - II**

SIGNAL MODELS: Amplitude model, Radar cross section, Statistical description, clutter: Noise model, Signal to Noise ratio, jamming. Frequency models: Doppler shift, Spatial Models, Variation with angel cross range multipath.

**UNIT - III**

SAMPLING AND QUANTIZATION OF PULSED RADAR SIGNALS: Domain criteria for sampling radar signals, sampling in the fast time dimension, Sampling in slow time, Sampling the Doppler spectrum, spatial and angel dimension, Quantization.

**UNIT - IV**

Radar Waveforms: Waveform Matched filter of moving targets Ambiguity function, Pulse burst Waveforms. Frequency Modulated pulse compression wave forms: Introduction, significance, Types. Linear FM Pulse Compression – Block Diagram, Characteristics reduction of Side Lobes, Stretch Techniques. Generation and decoding of FM Waveforms - block, schematic and characteristics of passive system, digital compression.

**UNIT - V**

DOPPLER PROCESSING: Moving Target Indication: Pulse cancellers, matched filters for clutter suppression, blind speeds Pulse Doppler processing: DFT of moving targets, Sampling of DTFT, Fine Doppler estimation. Pulse pair processing. Detection Fundamentals: Neynan – Pearson Detection Rule, Threshold Detection of radar signals.

**UNIT - VI**

PHASE CODING TECHNIQUES: Principles, Binary Phase Coding, Barker Codes, Maximal Length Sequences (MLS/LRS/PN), Block Diagram of a Phase Coded CW Radar. Linear FM and Frequency Coding Techniques: Principles, Linear FM pulses, Generation and Decoding, Distortion effects on LFM Signals, Discrete Frequencies, Waveform Analysis, Capabilities, Resolution properties of Frequency Coded Pulses.

**TEXT BOOKS:**

1. Mark. A. Richards, “Fundamentals of Radar Signal Processing”, TMH, 2005.

**REFERENCES:**

1. Fred E. Nathanson, “Radar Design Principles: Signal Processing and the Environment”, 2nd ed., PHI, 1999.

2. Peyton Z. Peebles Jr, “Radar Principles”, John Wiley, 2004.

3. R. Nitzberg, “Radar Signal Processing and Adaptive Systems”, Artech House, 1999.

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – I Sem.**

**HDL PROGRAMMING LABORATORY**

**(Common to M. Tech. VLSI and DECS)**

**Subject Code : 16MVL1101 Internal Marks: 40**

**Credits : 2 External Marks: 60**

**Objectives**

1. Study the Xlinx software.

2. Analyze and experience with principle of designing digital circuits

3. Simulate the digital circuits by using VHDL/Verilog.

4. Synthesize the digital circuits by using VHDL

5. Implement the digital circuits by using VHDL.

**Outcomes**

1. Simulate the digital circuits by using VHDL/ Verilog.

2. Synthesis and implement the digital circuits by using VHDL.

3. Generate RTL schematics and timing constraints.

4. Produce power report and Place and Route report of digital circuit synthesis.

5. Implement the digital circuits by using FPGA devices

**The students are required to simulate, synthesize and implement the following experimental part, on the VHDL/Verilog environment.**

1. Digital Circuits Description using Verilog and VHDL

2. Verification of the Functionality of Designed circuits using function Simulator.

3. Timing simulation for critical path time calculation.

4. Synthesis of Digital circuits

5. Place and Route techniques for major FPGA vendors such as Xilinx, Altera and Actel etc.

6. Implementation of Designed Digital Circuits using FPGA and CPLD devices.

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – II Sem.**

**SPREAD SPECTRUM COMMUNICATIONS**

**Subject Code : 16MDE1005 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives :**

1. To study about spread spectrum processing.
2. To analyse in detailed manner about different signals in spread spectrum communication system.
3. To understand about an acquisition and tracking process of spread spectrum communication system.
4. To explain receivers and filters for spread spectrum signals.
5. To explain benefits in bandwidth and energy parameters.
6. To explain applications of spread spectrum system.

**Outcomes:**

After completion of this course the students will be able to

1. Get an idea about spread spectrum signal processor.
2. Analyse about different hopping receivers.
3. Analyse and differentiate all generators in spread spectrum communication system.
4. Design spread spectrum communication system for an acquisition.
5. Design spread spectrum communication system for tracking.
6. Apply spread spectrum process in wireless distributed computing system.

**UNIT I**

INTRODUCTION ABOUT SPREAD SPECTRUM: General concepts, Brief analysis of Direct sequence (DS), Pseudo Noise (PN), Frequency hopping, and Time hopping, Hybrid Spread spectrum systems, and Chirp spread spectrum.

**UNIT II**

ANALYSIS OF AVOIDANCE – TYPE SPREAD SPECTRUM SYSTEMS: The frequency hopped signal, Interference rejection in a frequency hopping receiver, the time hopped signal.

**UNIT III**

GENERATION AND DETECTION OF SPREAD SPECTRUM SIGNALS: Shift register sequence generators, SAW device PN generators. Coherent direct sequence receivers.

**UNIT IV**

ACQUISTION OF SPREAD SPECTRUM SIGNALS: Acquisition of spread spectrum signals, Acquisition cell by cell searching, Reduction of Acquisition time, Acquisition with matched filters, Matched filters with acquisition – aiding Waveform.

**UNIT V**

TRACKING OF SPREAD SPECTRUM SIGNALS: Method of carrier tracking, Delay lock loop analysis, Tau – Dither loop, Coherent carrier tracking, Non coherent frequency hop receiver.

**UNIT VI**

APPLICATION OF SPREAD SPECTRUM TO COMMUNICATIONS: General capabilities of spread spectrum, Multiple access considerations, Energy and Bandwidth efficiency in multiple accesses, Selective calling and Identification, Antijam Considerations, Error correction coding.

**TEXT BOOKS**

1. “Modren Communications and Spread Spectrum”, George. R. Cooper and Clare D. McGillem,

McGraw hill Book Company.

2. “Introduction to Spread Spectrum Communications”, Roger L. Peterson, Rodger E. Ziemer &

David E. Borth, Prentice Hall 1995.

**REFERENCE BOOKS:**

1. “Wireless Digital Communications – Modulation & Spread Spectrum Applications”, Dr. Kamilo

Feher,PHI, 1999.

2. “Wireless Communication”, Upena Dalal, Oxford Higher Educatiion, 2009.

3. “Wireless Communications”, Andrea Goldsmith Cambridge University Press, 2005.

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – II Sem.**

**DETECTION AND ESTIMATION OF SIGNALS**

**Subject Code : 16MDE1006 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives:**

1. Understand basic estimation and detection background for engineering applications.
2. Understand algorithms of detection and estimation theory for practical applications.
3. Design and analyze optimum detection schemes.
4. Study different estimation schemes such as LMS and Bayes estimators.
5. Understand the basics of linear filtering.

**Outcomes:**

1. Analyze signal estimation in discrete-time domain using filters.
2. Examine the detection of deterministic and random signals using statistical models.
3. Apply estimation methods to real engineering problems.
4. Examine the performance of signal parameters using optimal estimators.
5. Generalize Classical and Bayesian Estimation Approaches
6. Demonstrate statistical decision theory used for signal detection and estimation

**UNIT – I**

INTRODUCTION TO DISCRETE-TIME SIGNALS: Fourier series representation and Fourier Transform of a discrete time signal. Examples: Amplitude and phase spectrum. Frequency content and sampling rates, Transfer function, Frequency response, problems.

**UNIT – II**

RANDOM DISCRETE-TIME SIGNALS: Review of probability – Random data: moments and histograms – Generation and shaping of pseudorandom noise. Filtered random signals – Autocorrelation and power spectral density – Sampling band limited random signals.

**UNIT – III**

OPTIMUM ALGORITHMS FOR DETECTION OF SIGNALS IN NOISE – 1: Minimum probability of Error. Criterion, Neyman – Person criterion for Radar, Applications to Air Traffic Control radar, detection of constant and variable – amplitude signals.

**UNIT – IV**

OPTIMUM ALGORITHMS FOR DETECTION OF SIGNALS IN NOISE – 2: Matched filters. Optimum formulation, detection of Random signals – Simple problems there on with multisampling cases.

**UNIT – V**

ESTIMATION OF SIGNALS IN NOISE: Linear mean squared estimation – Bayes estimator, its examples – Maximum likelihood estimate of parameters of linear system.

**UNIT – VI**

RECURSIVE LINEAR MEAN SQUARED ESTIMATION: Estimation of a signal parameter. Estimation of time-varying signals – Kalman filtering – Filtering signals in noise – Treatment restricted to two variable case only – Simple problems, Application to Air Traffic Control radar tracking.

**TEXT BOOK:**

1. Signal processing: Discrete Spectral analysis, Detection and Estimation, Mischa Schwartz and Leonard Shaw, Mc-Graw Hill Book Company, 1975.

**REFERENCE BOOKS:**

1. E.L. Van Trees, Detection, Estimation and Modulation Theory, Wiley, New York, 1968.
2. Shanmugam and Breipohl, „Detection of signals in noise and estimation‟, John Wiley & Sons, New York, 1985.
3. Srinath, Rajasekaran & Viswanathan, Introduction to statistical Signal processing with Applications, Prentice Hall of India, New Delhi, 110 001,1989.

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – II Sem.**

**WIRELESS COMMUNICATION & NETWORKS**

**Subject Code : 16MDE1007 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives :**

1. Understand wireless networking concepts
2. Explain about multiple access techniques and MAC channels
3. Describe the fundamental concepts of spread spectrum systems.
4. Elaborate the operation of mobile IP and WAP
5. Explain various types of WLAN
6. Describe Bluetooth and mobile data networks

**Outcomes:**

1. Explain about wireless networks
2. Describe various multiple access techniques and MAC channels for wireless communication
3. Analyze different type of spread spectrum systems
4. Explain the operation of mobile IP and WAP
5. Distinguish among various types of WLAN
6. Elaborate Bluetooth and mobile data network

**UNIT – I**

INTRODUCTION TO WIRELESS NETWORKING: Introduction, Difference between wireless and fixed telephone networks, Development of wireless networks, Traffic routing in wireless networks. Wireless data services: CDPD, ARDIS, RMD, Common Channel Signaling.

**UNIT – II**

MULTIPLE ACCESS TECHNIQUE & MAC CHANNELS FOR WIRELESS COMMUNICATION: Introduction, TDMA, FDMA, CDMA, SDMA ,Packet radio, Packet radio protocols, CSMA protocols, Reservation protocols, MAC channels, MAC channel capacity with fading and ISI.

**UNIT – III**

FUNDAMENTAL CONCEPTS OF SPREAD SPECTRUM SYSTEMS: pseudo noise sequence, analysis of DSSS systems - the processing gain and anti jamming margin - frequency hopped spread spectrum systems - time hopped spread spectrum systems - synchronization of spread spectrum systems

**UNIT – IV**

MOBILE IP AND WIRELESS ACCESS PROTOCOL: Operation of mobile IP, Co-located address, Registration, Tunneling, WAP Architecture, WAP service, WAP session protocol, wireless transaction, Wireless datagram protocol.

**UNIT – V**

WLAN TECHNOLOGY: Infrared LANs, Spread spectrum LANs, Narrow bank microwave LANs.

**UNIT – VI**

BLUE TOOTH AND MOBILE DATA NETWORKS: Overview, Radio specification, Base band specification, Links manager specification, Logical link control and adaptation protocol, Mobile data networks Introduction, Wireless ATM, HIPERLAN, Adhoc Networking and WPAN.

**TEXT BOOKS:**

1. Wireless Communications, Principles, Practice – Theodore, S. Rappaport, PHI, 2nd Edn., 2002.

2. Wireless Communication and Networking – William Stallings, PHI, 2003.

**REFERENCE BOOKS:**

1. Principles of Wireless Networks – Kaveh Pah Laven and P. Krishna Murthy, Pearson Education,

2002.

2. Wireless Digital Communications – Kamilo Feher, PHI, 1999.

3. Wireless Communications – Andreaws F. Molisch, Wiley India, 2006.

4. Introduction to Wireless and Mobile Systems – Dharma Prakash Agarwal, Qing-An Zeng,

Thomson 2nd Edition, 200

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – II Sem.**

**CODING THEORY & TECHNIQUES**

**Subject Code : 16MDE1008 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives:**

**The student will be able to**

1. Develop basic understanding of the extension field called Galois field and their role in the design of BCH and RS codes.
2. Understand the theoretical framework upon which error-control codes are built.
3. Know the mathematical structure of error correcting codes.
4. Implement some of the error-control codes discussed in class

**Outcomes:**

**At the end of the course the student will be able to**

1. Understand about the need and importance of channel coding methods.
2. Apply coding techniques in various communication systems like wireless communications to achieve a better coding gain.
3. Identify the problems in error control techniques.
4. Solved different error control problems
5. Learn different space- time codes.
6. Implement coding techniques in real time systems.

**UNIT –I:**

Coding for Reliable Digital Transmission and Storage: Mathematical model of Information, A Logarithmic Measure of Information, Average and Mutual Information and Entropy, Types of Errors, Error Control Strategies.

**UNIT –II:**

Linear Block Codes: Introduction to Linear Block Codes, Syndrome and Error Detection, Minimum Distance of a Block code, Error-Detecting and Error-correcting Capabilities of a Block code, Standard array and Syndrome Decoding, Probability of an undetected error for Linear Codes over a BSC, Hamming Codes. Applications of Block codes for Error control in data storage system.

**UNIT –III:**

Cyclic Codes: Description, Generator and Parity-check Matrices, Encoding, Syndrome Computation and Error Detection, Decoding ,Cyclic Hamming Codes, Shortened cyclic codes, Error-trapping decoding for cyclic codes, Majority logic decoding for cyclic codes.

**UNIT –IV:**

Convolutional Codes: Encoding of Convolutional Codes, Structural and Distance Properties, maximum likelihood decoding, Sequential decoding, Majority- logic decoding of Convolution codes. Application of Viterbi Decoding and Sequential Decoding, Applications of Convolutional codes in ARQ system.

**UNIT –V:**

Burst –Error-Correcting Codes: Decoding of Single-Burst error Correcting Cyclic codes, Single Burst-Error-Correcting Cyclic codes, Burst-Error-Correcting Convolutional Codes, Bounds on Burst Error-Correcting Capability, Interleaved Cyclic and Convolutional Codes, Phased-Burst –Error Correcting Cyclic and Convolutional codes.

**UNIT -VI:**

BCH – Codes: BCH code- Definition, Minimum distance and BCH Bounds, Decoding Procedure for BCH Codes- Syndrome Computation and Iterative Algorithms, Error Location Polynomials and Numbers for single and double error correction

**TEXT BOOKS:**

1. Error Control Coding- Fundamentals and Applications –Shu Lin, Daniel J.Costello,Jr, Prentice

Hall, Inc.

2. Error Correcting Coding Theory-Man Young Rhee- 1989, McGraw-Hill Publishing.

**REFERENCE BOOKS:**

1. Digital Communications-Fundamental and Application - Bernard Sklar, PE.

2. Digital Communications- John G. Proakis, 5th Ed., 2008, TMH.

3. Introduction to Error Control Codes-Salvatore Gravano-oxford

4. Error Correction Coding – Mathematical Methods and Algorithms – Todd K.Moon, 2006, Wiley

India.

5. Information Theory, Coding and Cryptography – Ranjan Bose, 2nd Ed, 2009, TMH.

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – II Sem.**

**VLSI SIGNAL PROCESSING**

**(Common to VLSI and DECS)**

**Subject Code : 16MVL1013 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives:**

1. Understand the pipelining and parallel processing techniques to the VLSI system
2. Analyze the retiming, unfolding & folding concepts for register minimization
3. Understand the systolic architectures
4. Understand the various arithmetic circuits for signal processing
5. Understand and apply the fast convolution algorithms for signal processing applications
6. Explain different low power algorithms.
7. Explain redundant number representation and numerical strength reduction algorithms.

**Outcomes:**

1. Design parallel processors in VLSI systems
2. Implement the register minimization using the retiming, unfolding & folding concepts.
3. Design systolic architecture using canonical mapping and generalized mapping.
4. Analyze the fast convolution algorithms and use them for signal processing applications
5. Design low power multipliers using bit level arithmetic circuits.
6. Design low power multipliers using multiple constant algorithms.

**UNIT – I**

Introduction to DSP :Introduction, Typical DSP algorithms, Representation of DSP algorithms , Iteration Bound-Data flow graph Representation, loop bound, iteration bound, algorithms for computing iteration bound, iteration bound of multirate dataflow graphs. Pipelining and Parallel Processing: Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power,

**UNIT – II:**

RETIMING: Introduction – Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNFOLDING: Introduction – An Algorithm for Unfolding – Properties of Unfolding – critical Path, Unfolding and Retiming – Applications of Unfolding

Folding: Introduction - Folding Transform – Register minimization Techniques – Register minimization in folded architectures – folding of multirate systems

**UNIT – III:**

Systolic Architecture Design: Introduction – Systolic Array Design Methodology – FIR Systolic Arrays – Selection of Scheduling Vector – Matrix Multiplication and 2D Systolic Array Design – Systolic Design for Space Representations contain delays.

**UNIT – IV:**

Fast Convolution: Introduction – Cook-Toom Algorithm – Winogard algorithm – Iterated Convolution – Cyclic Convolution – Design of Fast Convolution algorithm by Inspection

**A**LGORITHM STRENGTH REDUCTION FILTERS AND TRANSFORMS: Introduction, parallel FIR filters, Discrete cosine Transform and Inverse DCT

**UNIT – V:**

BIT-LEVEL ARITHMETIC ARCHITECTURES-Introduction, parallel multipliers, Interleaved floor plan and Bit plane based digital filters, Bit-Serial Multipliers, Bit-Serial filter design and implementation, Canonic Signed Digit Arithmetic, Distributed Arithmetic

**UNIT – VI:**

REDUNDANT ARITHMETIC: Introduction, Redundant number representation, Carry free Radix-2 Addition and Subtraction, Hybrid Radix-4 addition, Radix -2 Hybrid redundant multiplication architectures, data format conversion, redundant to non redundant converter

NUMERICAL SRENGTH REDUCTION: Introduction, Sub expression Elimination, Multiple constant multiplications, Sub expression sharing in digital filters, additive and multiplicative number splitting.

**TEXT BOOKS:**

1. Keshab K. Parthi, VLSI Digital Signal Processing- System Design and Implementation –1998,

Wiley Inter Science.

2. Kung S. Y, H. J. While House, T. Kailath, VLSI and Modern Signal processing, 1985, Prentice

Hall.

**REFERENCE BOOKS**:

1. Jose E. France, Yannis Tsividis, Design of Analog – Digital VLSI Circuits for Telecommunications and Signal Processing –1994, Prentice Hall.
2. Medisetti V. K, VLSI Digital Signal Processing, IEEE Press (NY), USA, 1995.

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – II Sem.**

**SYSTEM MODELING & SIMULATION**

**(Common to VLSI and DECS)**

**Subject Code : 16MVL1014 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives**

1. Analyze approaches to system modeling and simulation
2. Design simulation model for linear systems.
3. Develop simulation for motion control models.
4. Analyze state machine model
5. Develop Petri nets for a problem and its analysis
6. Analyze the simulation of queuing systems and optimization.

**Outcomes**

1. Analyze the given system or problem
2. Design a model to represent the system or problem
3. Develop simulation models for time and event driven systems
4. Analyze State machine models
5. Design simulation models for given system using petri nets
6. Analyze the queuing systems and optimization

**UNIT – I**

BASIC SIMULATION MODELING: Systems, Models and Simulation, Discrete Event Simulation, Simulation of Single server queuing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

**UNIT – II**

SIMULATION SOFTWARE: Comparison of simulation packages with Programming Languages, Classification of Software, Desirable Software features, General purpose simulation packages – Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

**UNIT – III**

BUILDING SIMULATION MODELS: Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

MODELING TIME DRIVEN SYSTEMS: Modeling input signals, delays, System Integration, Linear Systems, Motion Control models, numerical experimentation.

**UNIT – IV**

EXOGENOUS SIGNALS AND EVENTS: Disturbance signals, state machines, petri nets & analysis, System encapsulation.

MARKOV PROCESS: Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous –Time Markov processes.

**UNIT – V**

EVENT DRIVEN MODELS: Simulation diagrams, Queuing theory, simulating queuing systems, Types of Queues, Multiple Servers.

**UNIT – VI**

SYSTEM OPTIMIZATION: System identification, Searches, Alpha/beta trackers, multidimensional optimization, modeling and simulation methodology.

**TEXT BOOKS:**

1. System Modeling & Simulation, An introduction – Frank L. Severance, John Wiley & Sons, 2001.

2. Simulation Modeling and Analysis – Averill M. Law, W. David Kelton, TMH, 3rd Edition, 2003.

**REFERENCE BOOK:**

1. Systems Simulation – Geoffery Gordon, PHI, 1978.

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – II Sem.**

**ADAPTIVE SIGNAL PROCESSING**

**Subject Code : 16MDE1009 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives :**

1. To recall the fundamentals of eigen value and vectors concept
2. To study introduction to adaptive system
3. To study the searching for performance surface
4. To study the steepest descent algorithm
5. To study the concept of LMS & RLS algorithms

**Outcomes:**

1. Recall the mathematical concepts related to eigen value and vector concept.
2. Understand the need of adaptive system.
3. List applications of adaptive systems
4. Compare gradient search methods
5. Understand the concept of LMS algorithm
6. Distinguish LMS and RLS algorithms

**UNIT I**

EIGEN ANALYSIS: Eigen Value Problem, Properties of eigen values and eigen vectors, Eigen Filters, eigen Value computations.

**UNIT II**

INTRODUCTION TO ADAPTIVE SYSTEMS: Definitions, Characteristics, Applications, Example of an Adaptive System. The Adaptive Linear Combiner -Description, Weight Vectors, Desired Response Performance function, Gradient & Mean Square Error.

**UNIT III**

DEVELOPMENT OF ADAPTIVE FILTER THEORY & SEARCHING THE PERFORMANCE SURFACE: Introduction to Filtering, Smoothing and Prediction, Linear Optimum Filtering, Problem statement, Principle of Orthogonality – Minimum Mean Square Error, Wiener- Hopf equations, Error Performance - Minimum Mean Square Error.

SEARCHING THE PERFORMANCE SURFACE: Methods & Ideas of Gradient Search methods, Gradient Searching Algorithm & its Solution, Stability & Rate of convergence - Learning Curves.

**UNIT IV**

STEEPEST DESCENT ALGORITHMS: Gradient Search by Newton’s Method, Method of Steepest Descent, Comparison of Learning Curves.

**UNIT V**

LMS ALGORITHM & APPLICATIONS: Overview - LMS Adaptation algorithms, Stability & Performance analysis of LMS Algorithms - LMS Gradient & Stochastic algorithms, Convergence of LMS algorithm.

Applications: Noise cancellation, Cancellation of Echoes in long distance telephone circuits, Adaptive Beam forming.

**UNIT-VI**

RLS ALGORITHM: Matrix Inversion lemma, Exponentially weighted recursive least square algorithm, update recursion for the sum of weighted error squares, convergence analysis of RLS Algorithm, Application of RLS algorithm on Adaptive Equalization

**Text Books**:

1. Adaptive Signal Processing - Bernard Widrow, Samuel D.Strearns, 2005, PE.

2. Adaptive Filter Theory - Simon Haykin-, 4 ed., 2002,PE Asia.

**Reference Books:**

1. Optimum signal processing: An introduction - Sophocles.J.Orfamadis, 2 ed., 1988, McGraw-Hill,

Newyork

2. Adaptive signal processing-Theory and Applications, S.Thomas Alexander, 1986, Springer

Verlag.

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – II Sem.**

**SOFTWARE DEFINED RADIO**

**Subject Code : 16MDE1010 Internal Marks: 40**

**Credits : 4 External Marks: 60**

**Objectives :**

1. To study about benefits and different models for Software Defined Radio.
2. To study in detail about software defined radio architectures.
3. To get complete knowledge regarding functioning of different blocks and techniques associated with software defined radio.
4. To understand about power amplifiers, digital receivers and filters.
5. To analyse about conversion, linearity and non-linearity techniques.
6. To explain about range assignment techniques.

**Outcomes:**

After completion of this course the students will be able to

1. Get an idea about software defined radio and multi standard terminals.
2. Summarize the architectures of software defined radio.
3. Analyse and differentiate all amplifiers, transmitters and filters.
4. Design single and multi-carrier receiver systems.
5. Design multi band receiver and apply dynamic range assignment in radio systems.
6. Differentiate about linearity and non-linearity techniques and apply these techniques.

**UNIT I**

INTRODUCTION ABOUTSOFTARE DEFINED RADIO: Definition of Software defined radio, Benefits of multi-standard terminals, models for SDR, and its operation system.

**UNIT II**

ARCHITECTURE OF SOFTARE DEFINED RADIO: Software defined radio architectures, Hardware specifications, Digital aspects of Software defined radio, its limitations.

**UNIT III**

TRANSMITTERS: Flexible transmitters, Power amplifiers, Analogue quadrature up conversion, Interpolated band pass up conversion, PLL based modulator transmitter, All-pass filtering, Poly phase filtering.

**UNIT IV**

RECIEVRS: Flexible RF receiver architectures, Digital receiver, Single carrier and multi-carrier designs, Receiver sensitivity, ADC spurious signals.

**UNIT V**

RECIVER’S DESIGN: Multiband Flexible receiver design, RF Transmit / receive switch, Image rejection mixing, dynamic range enhancement.

**UNIT VI**

TECHNIQUES IN SOFTWARE DEFINED RADIO: Feed forward techniques, linearity, non-linearity techniques, their differences, its limitations and Applications.

**Text Books:**

1. Markus Dillinger, Kambiz Madani, Nancy Alonistioti, “Software Defined Radio: Architectures, Systems and Functions”, John Wiley & Sons, 2005.
2. Walter H.W. Tuttlebee, “Software Defined Radio: Enabling Technologies”, John Wiley & Sons, 2003.
3. Eugene Grayver, “Implementing Software Defined Radio”, Springer, 2012.

**Reference Books:**

1. P Kenington, “RF and Baseband Techniques for Software Defined Radio”, Artec House, 2005

2. JoukoVanakka, “Digital Synthesizers and Transmitter for Software Radio”, Springer, 2005

3. Wally H. W. Tuttlebee**, “**Software Defined Radio: Baseband Technologies for 3G Handsets and

Base stations”,John Wiley & sons , 2003

**Aditya Institute of Technology and Management, Tekkali**

**(Autonomous)**

**ELECTRONICS AND COMMUNICATION ENGINEERING**

**M.Tech (DECS) – II Sem.**

**Advanced Communication Laboratory**

**Subject Code : 16MDE1101 Internal Marks: 40**

**Credits : 2 External Marks: 60**

**Course Objectives:**

1. To design and verify the concepts of modern digital communication systems that operates from MHz-GHz range
2. To understand practical illustrations of various Digital Modulation and Demodulation techniques
3. To study the characteristics and various optical fiber parameters using different types of optical cables in single and multi-mode
4. To understand basic antenna types and their radiation patterns
5. To facilitate the student to become familiar with active & passive microwave devices & components used in Microwave communication systems

**Course Outcomes:**

1. Design of various Digital Modulation techniques
2. Examine how communication is being established using fibers in optical communications.
3. Examine characteristics of various antennae and its coverage area
4. Interpret characteristics and various losses associated with OFC channel
5. Compute the various microwave measurements

**List of Experiments**

1. Quadrature Phase Shift Keying Modulation and Demodulation using MATLAB
2. BER Simulation of DPSK modulation using MATLAB
3. BER comparison of different M-ary QAM with AWGN fading using MATLAB
4. Implementation of linear and cyclic codes using MATLAB
5. ASK generation and detection using MATLAB
6. FSK generation and detection using MATLAB
7. PSK generation and detection using MATLAB
8. Lease Mean Square (LMS) Algorithm using MATLAB
9. Analog and Digital communication link using optical fiber
10. Reflex klystron mode study
11. Study of Propagation loss, Bending loss and Measurement of Numerical Aperture in OFC
12. Measurement of frequency, guide wavelength, power, VSWR and attenuation in a microwave test bench.